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CONTROLLED INVERSION DEVICES

Sperry Research Center

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CONTROLLED INVERSION DEVICES

Harry Kroger

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Application and theory of Inversion Controlled Switch (ICS) devices (which we previously called "Controlled Inversion Devices") were investigated. Random access memory arrays of discrete devices were constructed in order to test memory array design. Each memory cell had only a single active device. Examination of the current voltage characteristics of the ICS memory cell and experiments on 3 x 3, 1 x 5 and 5 x 1 arrays lead to several refinements of cell design, the most important one being the use of diode isolation of device bases. This final circuit design effectively prevented all unwanted interactions

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between different memory cells. Using the circuit design a simple 2 x 2 integrated array was designed. The integrated circuit made use of buried layer emitter, junction isolation and amorphous germanium load resistors which were deposited directly on top of device collector contacts. The basic ICS structure chosen for this circuit were nolybdenum-SiO_2-n-p^+ devices. The circuit fabrication required seven masking steps including the one required to define the buried emitters. Fabrication studies revealed that most difficulties encountered were due to steps which were not connected with the active ICS device itself. Six wafers were processed. The final wafer had 100% yield except for damages incurred in probing. The array worked as expected as a static memory with non-destructive read out. Read, write and erase functions could be accomplished with only small incremental power requirements above that needed for holding information. The integrated circuit was designed with large areas to avoid fabrication difficulties. The power density required to hold information in the array devices was 14 watts per square centimeter of collector area. Projected performance of smaller area devices in larger arrays predicts that the holding total power could be as low as 5 mW for a 16K bit memory. Capacitance as a function of voltage was studied to help define band surface structure and to elucidate theory. It was noted that discrete devices could react nonlinearly to microwave frequency power and thus be used as microwave detectors or alarms. A variety of ICS structures were subjected to radiation hardness testing at RADC's Hanscom Field facilities using a 1MeV electron beam. Most devices could not hold information in a memory cell circuit when the transient dose rate was in the range of 5×10^8-10^9 rads (Si)/s. However, one structural variation, a nolybdenum-silicon oxynitride -p-n^+ structure could withstand transient radiation in the range of 10^{10} rads (Si)/s. Tests on other structural variations of this basic device type confirmed these results. The behavior under radiation and the effects of radiation hardening on memory cell circuit parameters can be predicted semi-quantitatively from the dc behavior of the device under full three-terminal biasing.

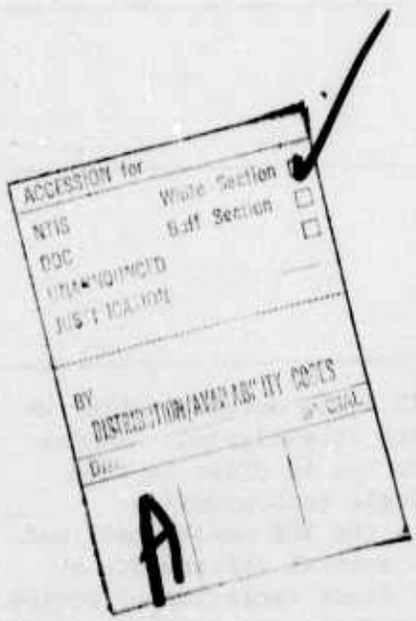

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

SECTION 1

INTRODUCTION

A. GOALS OF PROGRAM

The goals of this program are to:

(a) Complete basic theory of ICS operation;

(b) Study nonlinear, thin insulator conductors;

(c) Investigate ICS memory arrays;

(d) Investigate ICS logic circuits;

(e) Investigate problems of complete integration;

(f) Perform feasibility demonstration of complete integrated circuit;

(g) Investigate discrete device applications of ICS.

B. OUTLINE OF REPORT

The "inversion controlled switch" (ICS) is a novel semiconductor device which can exist in two stable conduction states, even though it has only one p-n junction. The type of structure investigated are shown in outline in Fig. 1. At the time of the award of this contract, the device was called a "controlled inversion device" but the obvious acronym (CID) could cause confusion with "charge injection device," to which the ICS bears no functional relationship.

The goals of this program have been met. Basic device properties and a theory sufficient for understanding applications have been completed and will be published. Appendices A and B are preprints of this basic material which also includes the most important properties of insulator materials which have been used in ICS devices.

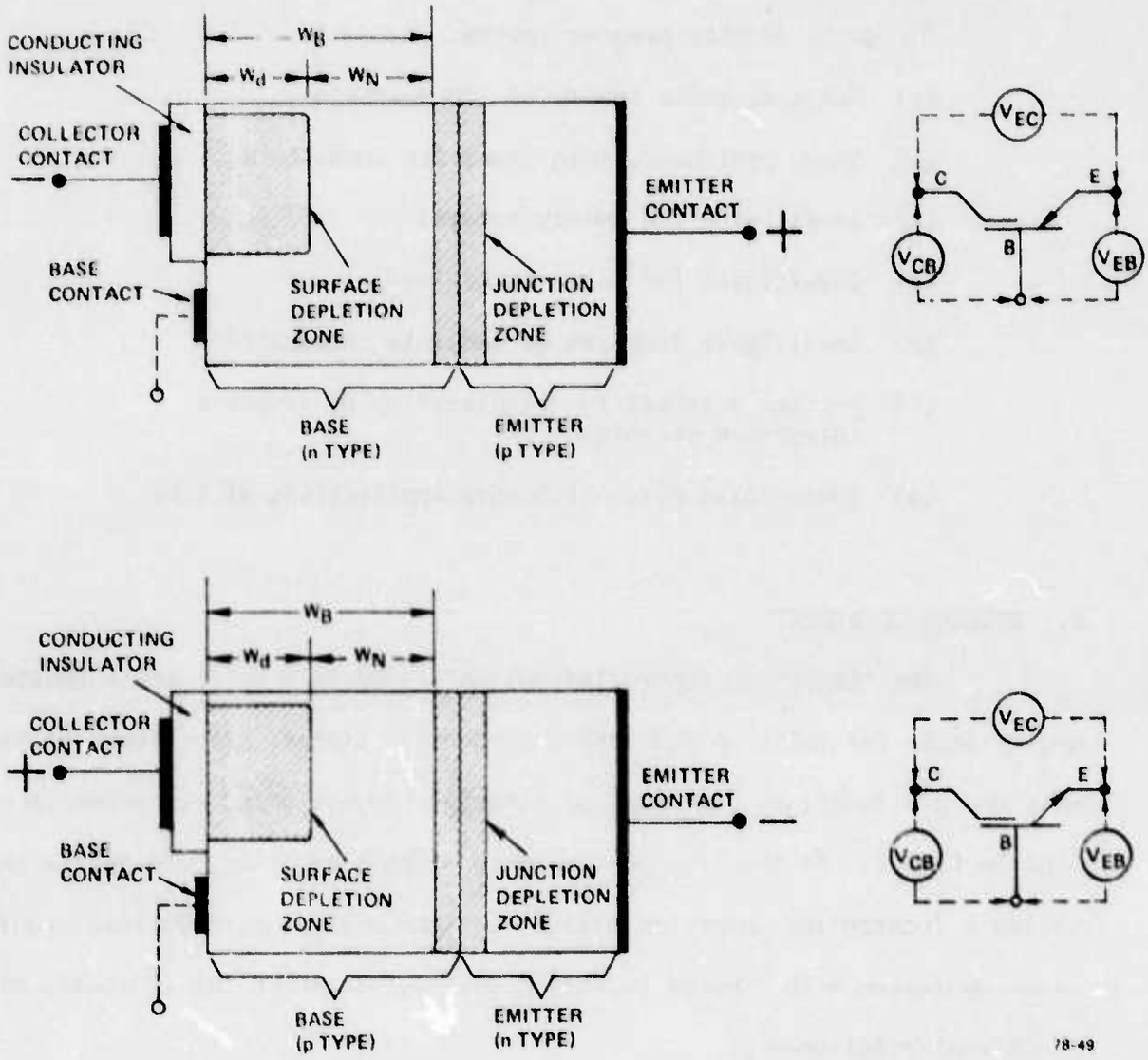

FIG. 1 Cross sectional diagram of basic inversion-controlled switch structures and circuit symbols.
Top: M-I-n-p structure.
Bottom: M-I-p-n structure.

ICS memory arrays have been investigated and are described in Secs. 2 and 3 of this report. The fabrication of small integrated arrays is described in Sec.3, and the projections on their potential future performance is presented in Sec. 4. Logic (nonlatching) circuits are described in Sec. 5. Section 6 describes the capacitance voltage characteristics of the devices and the relation of these measurements to basic device phenomena. An example of a potential discrete device application as a microwave detector or alarm is given in Sec. 7.

During the first contract on this device, an unexpected phenomenon was discovered in polycrystalline silicon. This was a nonvolatile memory switching characteristic. This phenomenon was not investigated to any substantial extent in the current contract because it proved to be a nonrugged device which was not radiation hard. Appendix C summarizes the previous work and the conclusions formed during the current contract.

Beyond the planned contract work the conventional ICS devices were examined for radiation hardness using RADC's LINAC accelerator at Hanscom Field. One version of the ICS device which had a silicon oxynitride insulator was exceptional with respect to its radiation hardness being able to withstand radiation doses of the order of 10^{10} rads(Si)/s without loosing information in a memory circuit. A report of these measurements with a preliminary interpretation is given in Appendix D.

SECTION 2

RAM MEMORY ARRAYS WITH RESISTIVE ISOLATION

A. INITIAL OPERATION OF RAM CIRCUITS

The first RAM circuits which were operated using small numbers of discrete ICS devices were simple ground-emitter and grounded-base circuits shown in Figs. 2 and 3. Fabrication of 2 x 2 and 3 x 3 element arrays using discrete devices was accomplished and the arrays operated using several types of ICS devices. Study of these circuits indicated that they were less than ideal because unless specially selected devices were used, the obvious extension of the circuit to N x N arrays would not be possible for $N \gtrsim 10\text{-}20$. The problem was interaction among devices in the same row. The threshold voltage of a device would depend slightly upon the number of other devices in the same row which were already in their low impedance state. As the number of devices in their low impedance state increased, the threshold voltage of the remaining devices would decrease and eventually fall below the voltage which must be supplied to the devices to hold information in the array. If a sufficient number of devices of one row were in their low impedance state the circuit would require all remaining devices of that row to be in their low impedance state, a situation clearly disastrous for memory applications. An improved circuit, which offers increased isolation along rows of the array, has been operated and permits more convenient readout of information without requiring the devices to be in a grounded-base configuration which increases the power dissipation.

B. IMPROVED MEMORY ARRAY

1. Basic Principles

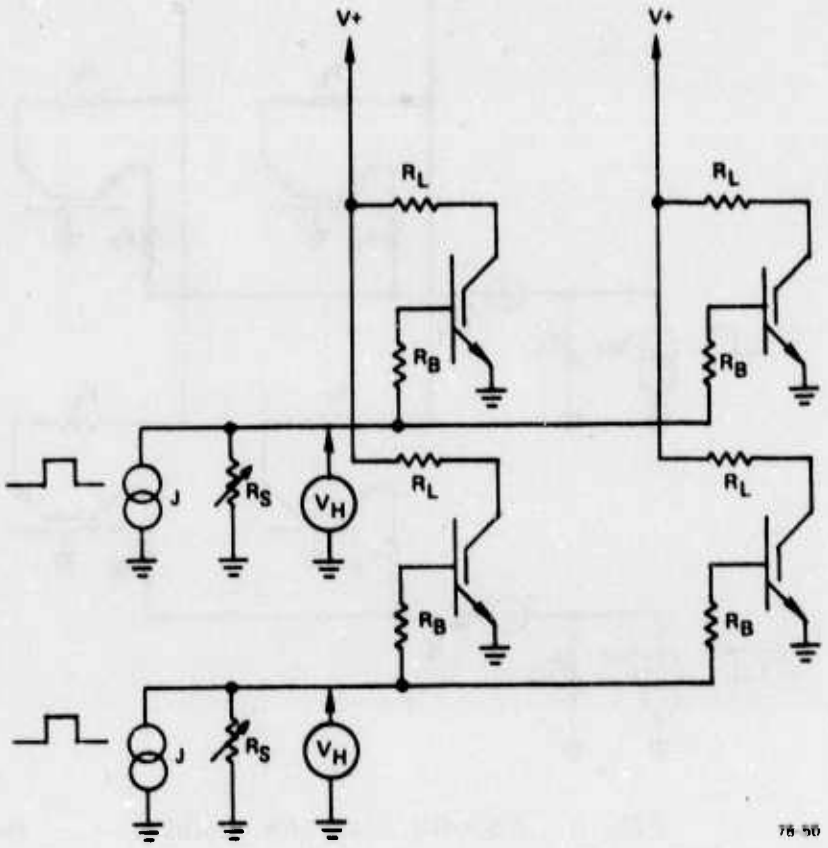

FIG. 2 Grounded emitter RAM circuit.

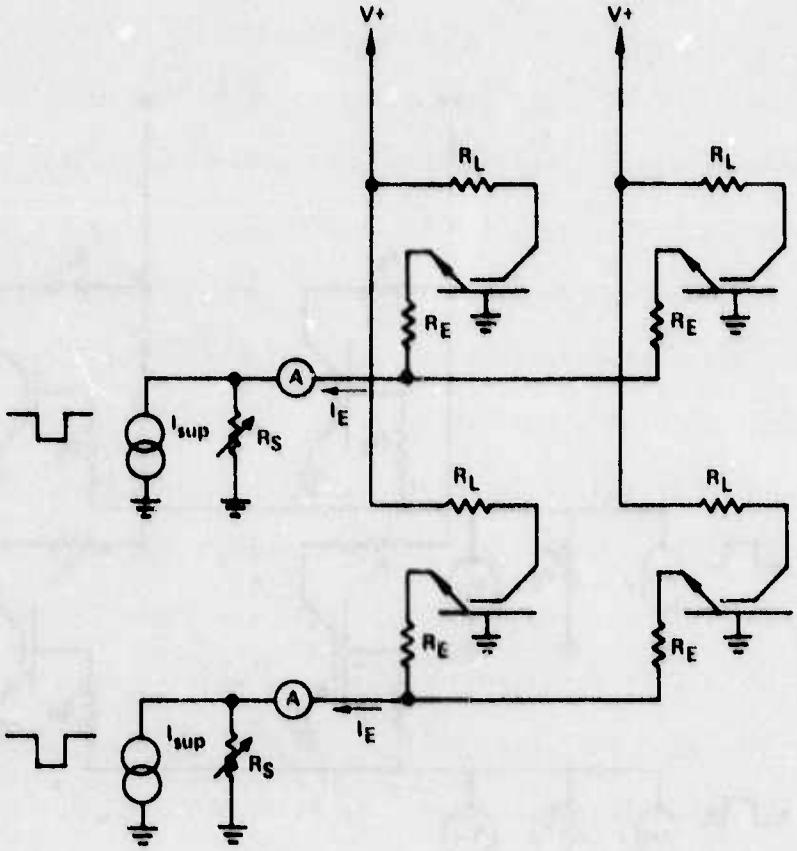

FIG. 3 Grounded base RAM circuit. 78-61

(a) Relevant two-terminal device properties. Bistable[1-4] and tristable[5] impedance states have previously been described in metal/conductive "insulator"/p-n junction devices when voltage is applied in the sense which tends to forward bias the p-n junction and deplete the semiconductor surface adjacent to the insulator. Figure 1 illustrates the basic device structure which is drawn for the more interesting case of three-terminal devices. The multiple impedance states are explained by a model of inversion-controlled conduction[2,3,5] which associates the existence of a high impedance state with a deep depletion of the semiconductor surface and a low impedance state with an existance of an inversion layer and consequent narrower surface depletion layer. The presence of an inversion layer permits a higher electric field to be impressed across the insulator than could be obtained at even a higher voltage across the entire device if no inversion layer were present.[2] Since current injection into or through the insulator is a nonlinear function of surface electric field, e.g., tunneling,[1] Schottky or Poole-Frenkel injection,[2] the current carried when an inversion layer is present can be many orders of magnitude greater when an inversion layer is present.[2]

The required properties of the insulator are: (1) It must be conductive enough to permit deep depletion of the semiconductor if large concentrations of minority carriers of the semiconductor surface layer are not injected into that region, and (2) Resistive enought to permit at least a partial build up of an inversion layer if the adjacent p-n junction is strongly forward biased.[2,3]

(b) Three-terminal device properties. The RAM circuit, which is the subject of this section, depends upon the more interesting properties of three-terminal devices which have been diagrammed in Fig. 1, in which electrical correction is made to both the metal and to the both sides of the p-n junction.

The "emitter," "base" and "collector" regions of the device have been previously defined; these terms suggest the similar functions each of these regions perform compared to those of a conventional bipolar transistor.[3]

It is useful to define certain current and voltage levels of two-terminal devices.[5] These critical currents and voltages will be seen to be functions of the biasing of three-terminal devices and of impedances which are placed between the emitter and base terminals of transistor structures. The threshold voltage V_{TH} is the highest voltage which may be placed on the devices in its high impedance state; the sustaining current I_S is the lowest current for which the low impedance is stable; the sustaining voltage V_S is the voltage across the device when the current through the device is equal to I_S. These critical currents and voltages are defined graphically in Fig. 4 which, by implication, assumes that only a high and low impedance state of the device is obtained. Many devices do not evidence a third, intermediate impedance state, and even for those devices which do not have an intermediate state, the appropriate choice of a low value of collector load resistance will suppress its appearance,[5] a situation which is also beneficial for minimum power consumption for memory applications as will be described below.

The values of V_{TH}, I_S and V_S can change if electrical connection is made to all three terminals of the device. These changes are: (1) the decrease of V_{TH} if the emitter junction forward biased;[3,5] (2) an increase in I_S if a conductance is added in shunt to the emitter and the terminals;[5] and (3) an increase in V_S for certain device structures if a shunt conductance is added to shunt the emitter and base terminals.[5] The observed variation in V_{TH}, I_S and V_S are all consistent with the inversion-controlled conduction model of device behavior.[2,5] These properties of one of the specific device structures which have been used in the RAM array are illustrated in Figs. 5 and 6.

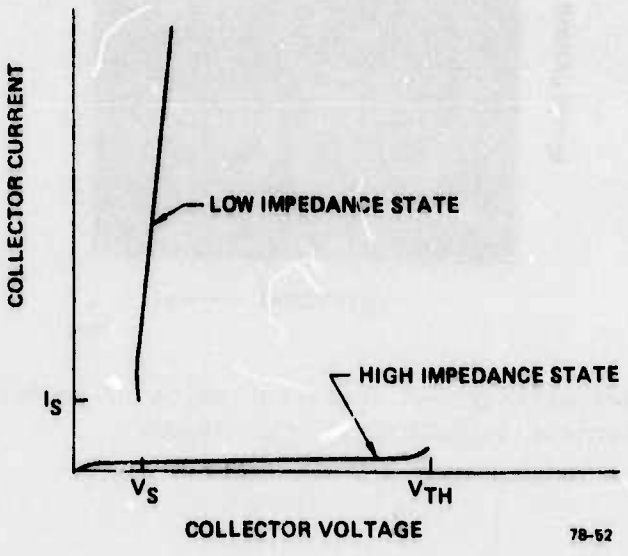

FIG. 4 Current-voltage characteristics of ICS, including graphical definitions of tnreshold voltage V_{TH}, sustaining voltage V_s and sustaining current I_s.

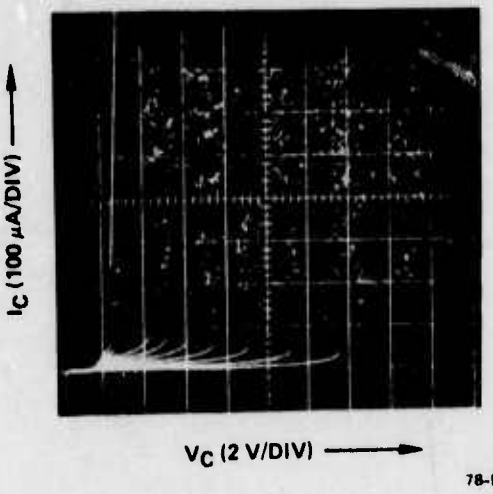

FIG. 5 Grounded emitter I-V characteristics of Mo-SiO_2-n-p^+ ICS with base current increased in 5 μA steps.

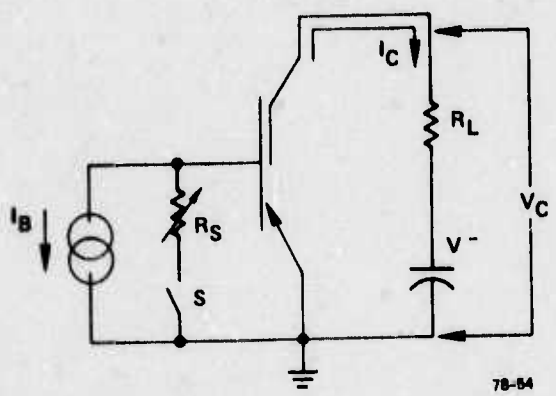

FIG. 6 Circuit used to obtain three-terminal I-V data. Switch S is open for data of Fig. 5; switch S is closed for data of Fig. 7.

Figure 5 presents collector-emitter current-voltage (I-V) characteristics for a $M/SiO_2/n/p^+$ device when the base current was raised in increments of 5 μA, from 0 to 30 μA. Note that the threshold voltage is suppressed from 13.5 V to 4 V. Figure 6 presents, in an expanded scale, the grounded-emitter output characteristics of the same device as a function of the resistance applied between the base and emitter terminals. The grounded emitter output characteristics of the same device as a function of the resistance applied between the base and emitter terminals. The circuit used to obtain these data is shown in Fig. 7. Note that I_S is increased by more than a factor of ten from less than 0.2 mA to 3.5 mA and that V_S is increased from 2.2 V to 4.4 V.

2. RAM Circuit Layout

The circuit of Fig. 8 is one arrangement drawn for a M/I/n/p structural variant which can be used as a static random-access memory (RAM) with NDRO. The particular circuit-device combination described is not optimized with respect to power consumption nor convenience of decoding, but does permit a simplified explanation of the operation. The devices operate essentially in a grounded-emitter configuration since the resistance R_E placed between emitter rows and ground is the lowest impedance level of the circuit. Note, however, that the emitter rows are mutually isolated from each other.

Information is stored as a binary 1 if the device is in its low impedance state and as a binary 0 if the device is in its high impedance state. A breadboard 3 x 3 array has been fabricated and tested using both $M/SiO_2/n/p^+$ and $M/SiO_xN_y/p/n^+$ discrete devices which had only two stable impedance states. An arbitrary pattern of 1's and 0's could be written into the array and the information stored at a selected site of the array could be read out correctly.

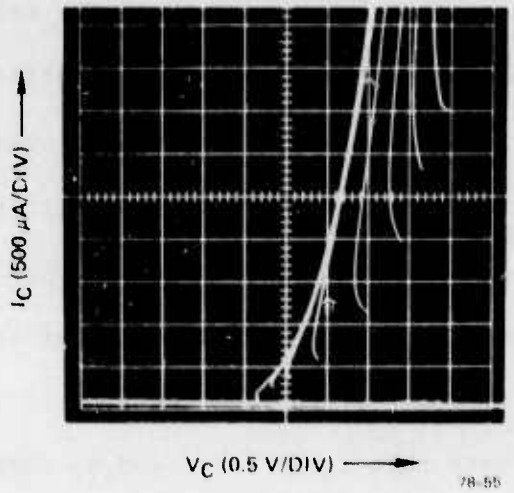

FIG. 7 Grounded emitter characteristics of Mo-SiO_2-n-p^+ device with $R_s = \infty$, 10 K, 4 K, 2 K, 500, 200 and 0 Ω. As R_s decreases, I_s and V_s increase.

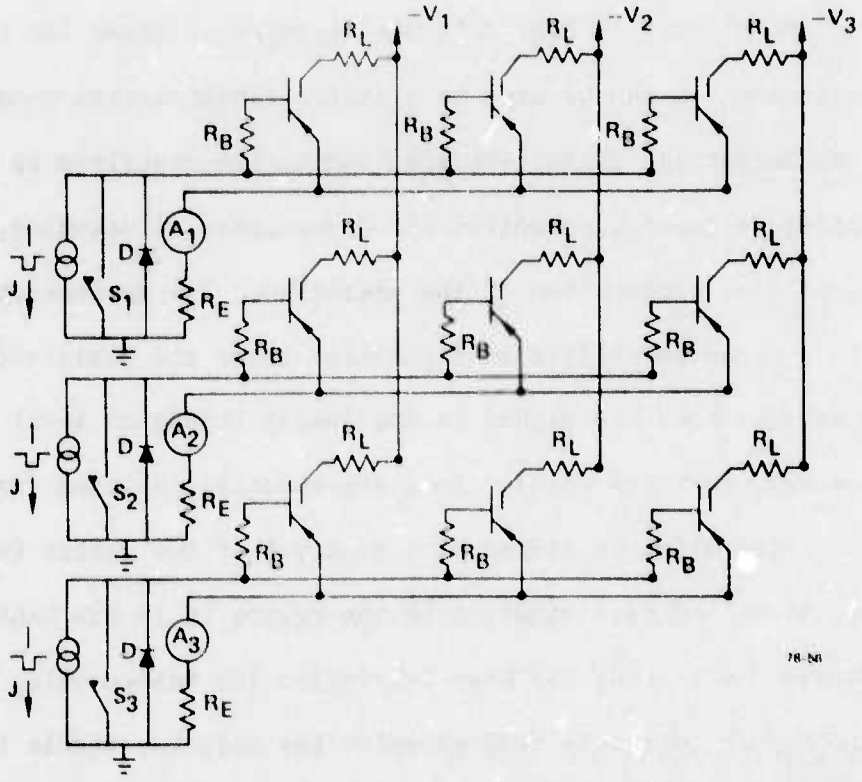

FIG. 8 Circuit diagram of 3 x 3 RAM array with isolated emitter and base rows.

3. Operation of the RAM Circuit

The operations of writing (changing a selected device from its high to low impedance state), erasing (changing a selected device from its low to high impedance state) and reading (determining in which state a selected location resides) can be carried out by procedures which follow directly from the discussions of Sec. 2B1. Throughout the discussion of how these operations can be performed, it will be assumed that the quiescent voltage V_q applied to all columns of the array is sufficiently large to hold all devices in their low impedance states regardless if any of the switches S_1, S_2 or S_3 are closed. This assumption does not result in the minimum holding power for the array but greatly simplifies the description of the required procedures.

(a) Write operation. A selected device, say, the one in the i^{th} row and j^{th} column, can be transferred from its high to its low impedance state without disturbing the rest of the array by the following operation:

(1) A current I_o is applied to the i^{th} base row, resulting in a current I, to each device.

(2) The voltage applied to the j^{th} column is raised above $V_{TH}(I_B = I)$; all other column voltages V_k for $k = j$ are left at $V_k = V_q$.

The array is restored to its holding state with the $(i-j)^{th}$ device now in the low impedance state, by undoing the above operations:

(3) V_j is reduced back to V_q, and

(4) The current I is withdrawn from the i^{th} row.

It is convenient and would consume less energy to write either an entire row or an entire column simultaneously rather than writing each bit sequentially. The natural word organization is by column rather than by row for the array of Fig. 8, since the erase and read operations to be described

are more conveniently performed by column than by row.

(b) Erase operation. A selected device, say the one in i^{th} row and j^{th} column, can be transferred from its low to its high impedance state without disturbing the rest of the array by the following procedure:

(1) Close switch S_i, leaving all other switches open.

(2) Reduce the supply voltage in the j^{th} column from V_q to a value V_j such that

$$V_S(R_{EB} \approx \infty) < V_j < V_S(R_{EB} = R_B)$$

The array is restored to its quiescent state (but now with the $(i-j)^{th}$ device in its high impedance state) by undoing the above operations:

(3) V_j is raised to V_q, and

(4) S_i is reopened.

To erase an entire column, it is only necessary to drop the voltage to below V_S. A word erase is attractive since actually less energy is dissipated on the array during the word erase than required to hold information in the array.

(c) Read operation. It is possible to determine the impedance state of a selected (say the $i\text{-}j^{th}$) device by the following procedure:

(1) Increase the voltage on the j^{th} row, and

(2) Measure variation of current in the i^{th} ammeter.

The current variation in the ammeter will be substantially larger (by a factor of 10^2-10^4, depending upon voltage pulse duration) if the $i\text{-}j^{th}$ device is in its low impedance state. The delay encountered at the device itself should be substantially less than 100 ps, since microwave network analyzer measurements show that the impedance level of the high impedance state is

$\approx 10^2$ times that of the low impedance state up to at least 10 GHz.[7]

It is also convenient to read out the information in an entire column simultaneously by examining the output of all ammeters rather than just one. No more power need be dissipated within the array to accomplish an entire word reading than is required to read a single bit. Neither the word nor bit readout will destroy information in the array.

4. Impedance Levels of RAM Circuit

An important impedance level of the circuit is $Z_o = V_S/I_S$. For the particular $M/SiO_2/n/p^+$ devices studied in this circuit $V_S = 2$ V and $I_S = 500\ \mu A$, thus, $Z_0 = 4 \times 10^3\ \Omega$. (These devices were examined because their I_S is proportioned to area; the particular devices had an active collector area of $1.3 \times 10^{-4}\ cm^2$. Thus, significantly higher values of Z_0 would result for smaller area devices.) The circuit is operated with resistances R_L and R_B such that $R_L/Z_0 \ll 1$ and $R_B/Z_0 \ll 1$. The operation of the circuit is described in detail below for the particular choices of $R_B = 100\ \Omega$, $R_L = 120\ \Omega$, and $R_E < 3\ \Omega$.

Information is stored on the array by applying a holding current $I_C = fI_S$ to the collector of every device which is in its binary I state. For $f < 5$, $V_C \approx V_S$. The power P dissipated in each memory site in which a 1 is stored is therefore

$$P = fV_SI_S + R_L(fI_S)^2 + R_BI_B^2 \quad , \qquad (1)$$

where I_B is the base current. The three terms of Eq. (1) represent the power dissipated in the active device, in the collector load resistance R_L and the base resistance R_B, respectively. The ratio of the second term to the first

is fR_L/Z_0. Since reliable operation can be obtained with $f \approx 2$, the power dissipated in the load need only be 6% of that dissipated in the active device. The power consumption in the base resistance is completely negligible since $I_B/I_C \ll 1/10$. For the devices used $P \approx 2$ mW; for similar devices which have a collector area of 1.6×10^{-7}, an easily obtainable size with conventional technology, one would expect a holding power requirement of only 2.5 μW per memory site. For other devices with smaller sustaining current densities and sustaining voltages, small area devices can be expected to require a power input of less than 1 μW per bit.

5. Static Isolation of Memory Elements

The presence of the base resistance R_B is, by itself, not generally sufficient to ensure adequate isolation of the memory elements in the array in order to guarantee proper operation. While increasing the value of R_B will improve isolation among the individual devices, such a procedure has limited utility since (without a major revision of the circuit) this will impose a lower limit on the emitter-base resistnace if the switches S_i are closed. This will be seen to be a hindrance to performing the "ERASE" operation as described above. The addition of the diode D, connected between the base rows and ground, together with the base resistance R_B, provide adequate isolation.

The inclusion of the diodes has several consequences. The major effect on an individual device is to raise its threshold voltage which would be expected for any finite conductance between emitter and base, as described in Sec. 2B1. To ensure good performance for the array, an emperical rule has been evolved which approximately relates the threshold voltage with diode present V_D, to the "infinite impedance" threshold voltage V_{TH}, and the "zero impedance" threshold voltage V_0:

$$V_D \approx \sqrt{V_{TH} V_O} \quad . \qquad (2)$$

Without the diodes in the circuit, the threshold voltage of a given device would be reduced additively for every other device in the same row which is already in its low impedance state.

On the other hand, the inclusions of the diodes significantly reduce the effect of low impedance devices on the threshold voltages of other devices in the same row. The presence of the diode prohibits the potential of the base row from being lowered more than approximately 0.5 V with respect to ground, no matter how many other devices are conducting. The addition of the emitter resistance R_E causes the emitter potential to be brought even closer to that of the bases and further reduces the change in V_{TH} of devices which are not in their low impedance state. By proper choice of the area of the diode and R_E the value of V_{TH} can be made essentially independent of the number of other devices in the row which are already in their low impedance state. Figure 9 shows the I-V characteristics of one device in a row of five devices, of the same type used in the 3 x 3 array. The circuit shown in Fig. 10 was used to obtain these data with no applied base current. Note that the threshold voltage of the devices changes less than 10%, independent of the number of other devices (0, 1, 2, 3, 4) which are already in their low impedance state, and that after at least one other device in the row is conducting, further changes in the selected device's threshold voltage are very small.

6. Dynamic Isolation of Devices Within a Row

The presence of the diodes D is important for this operation. Figure 11 shows the threshold voltage of the device in a five-element row of devices

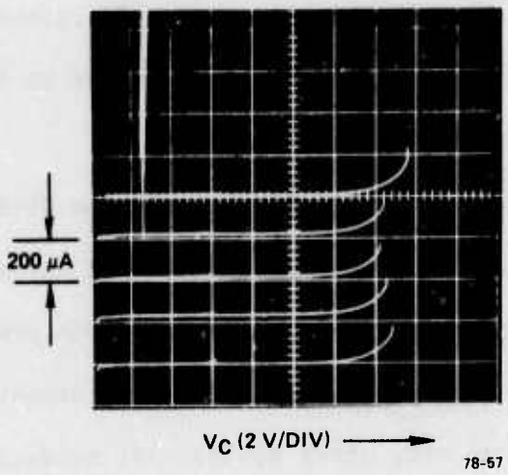

FIG. 9 I-V characteristic of device in row with four other devices with zero base current applied. Offset curves are for 0, 1, 2, 3 and 4 other devices in low impedance state. (Top trace is for no device in low impedance state.)

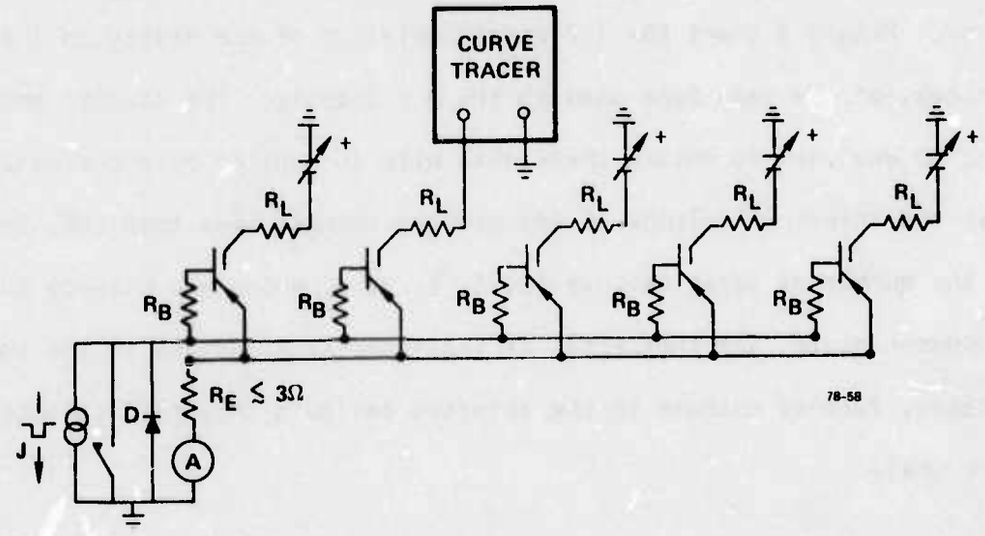

FIG. 10 Circuit used to determine I-V characteristics of a single device in a five-element row.

when a base current is applied to the base row circuit and when 0, 1, 2, 3 and 4 other devices are in their low impedance state. The circuit of Fig. 6 was again used to obtain these data but now with a base current applied. Note that the threshold voltage is significantly lower than those shown in Fig. 9 when no base current was applied. Furthermore, there is a negligible variation in threshold voltage as the number of other devices in the row are switched into their low impedance state. Without the presence of the diode this dynamic isolation would not be obtained in such a simple circuit.

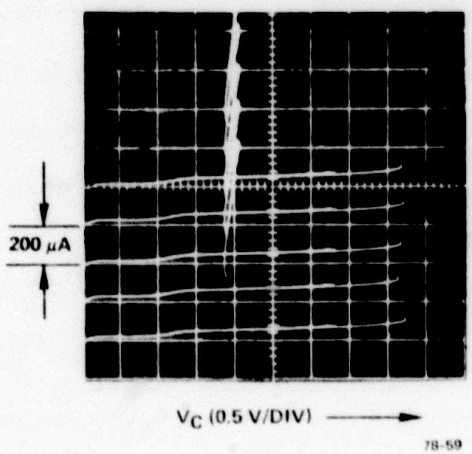

FIG. 11 I-V characteristics of device in row of five devices with 3 mA applied to base row. Offset curves are for 0, 1, 2, 3 and 4 other devices in low impedance state. (Top trace is for 0; bottom trace for 4 low impedance state devices.)

SECTION 3

RAM CIRCUITS WITH DIODE ISOLATION

A. FURTHER ANALYSIS OF UNWANTED INTERACTION

The interaction between devices in the same row is caused by currents I_{BL} which enter the base terminals of low impedance state devices, as shown in Fig. 12. These currents are in the opposite direction to those used to perform the WRITE operation, and in the opposite sense to conventional bipolar transistor base current. If these currents are largely supplied by currents I_{BH} which flow through base terminals of other devices in the same row which are in their high impedance state, then these high-impedance-state devices receive a forward bias to their emitter-base junctions. Note that the base current I_{BH} imposed on devices in their high impedance state is in the conventional sense for reducing threshold. The tendency for devices in their low impedance state to lower the threshold voltage of devices in the same row which are in their high impedance state is therefore explained.

The utility of the row shunt diode of Fig. 8 is also explained by these considerations. The forward conductance of the diode is so low that no significant current is drawn from the base terminals of any high-impedance-state devices. This situation, according to the terminology of Fig. 12, requires

$$I_D \approx \Sigma I_{BL} \; ; \; |I_{BL}| \gg I_{BH}$$

Several experimental relationships between the various currents and voltage drops across an ICS device are presented to quantify the above

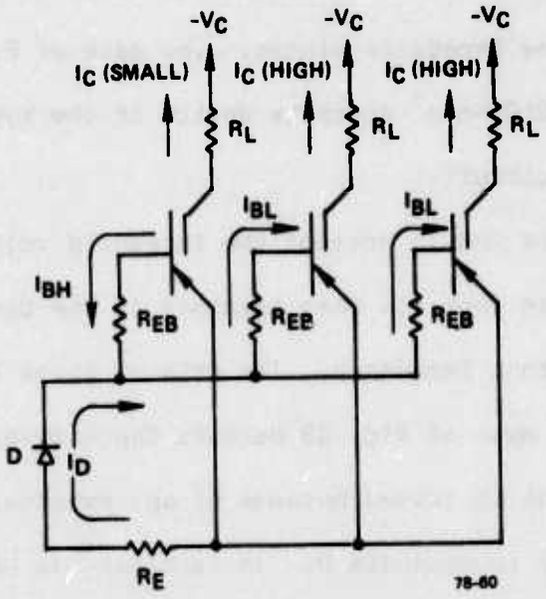

FIG. 12 Circuit diagram of 3-element row of memory array. Note different directions of base current for devices in high and low impedance states.

explanation. First, the critical voltage $(V_{EB})_{crit}$ across the emitter-base terminals of an ICS at threshold is essentially independent of external emitter-base shunt conductance. This fact enables the calculation of total current which must be supplied to the parallel combination of emitter-base terminals and external shunt conductance in order to initiate a transition from the high to low impedance states. The data of Fig. 13 were obtained from a molybdenum-SiO_2-n-p^+ discrete device of the type planned to be used in the integrated circuit.

Figures 14 and 15 present the threshold voltage V_{TH} as a function of the current drawn from the base terminal of the device when it is shunted by an external impedance. The data of these figures is not explicitly derivable from the data of Fig. 13 because the threshold voltage at zero applied base current is raised because of any external shunt conductance as described in detail in Appendix B. It is clear, as expected, that any finite shunt conductance will force a larger supply current to suppress the device's threshold voltage to a given value. It is also clear that a shunt diode will raise $V_{TH}(I_S = 0)$, a smaller amount than for any "interesting" value of R_S, since the desired values of R_S for these devices are in the range from 50-250 Ω. This observation is the first reason for preferring a diode shunt to a resistance in order to achieve isolation of individual base terminals in the memory array.

The behavior of base current when the device is its low impedance state is shown in Fig. 16. Note that in this figure a negative value of I_B implies that the base current enters the device and thus tends to increase the magnitude of the collector current. It is this phenomenon which is responsible for the interaction between low-impedance-state and high-impedance-state devices within the same row in the memory array. Larger

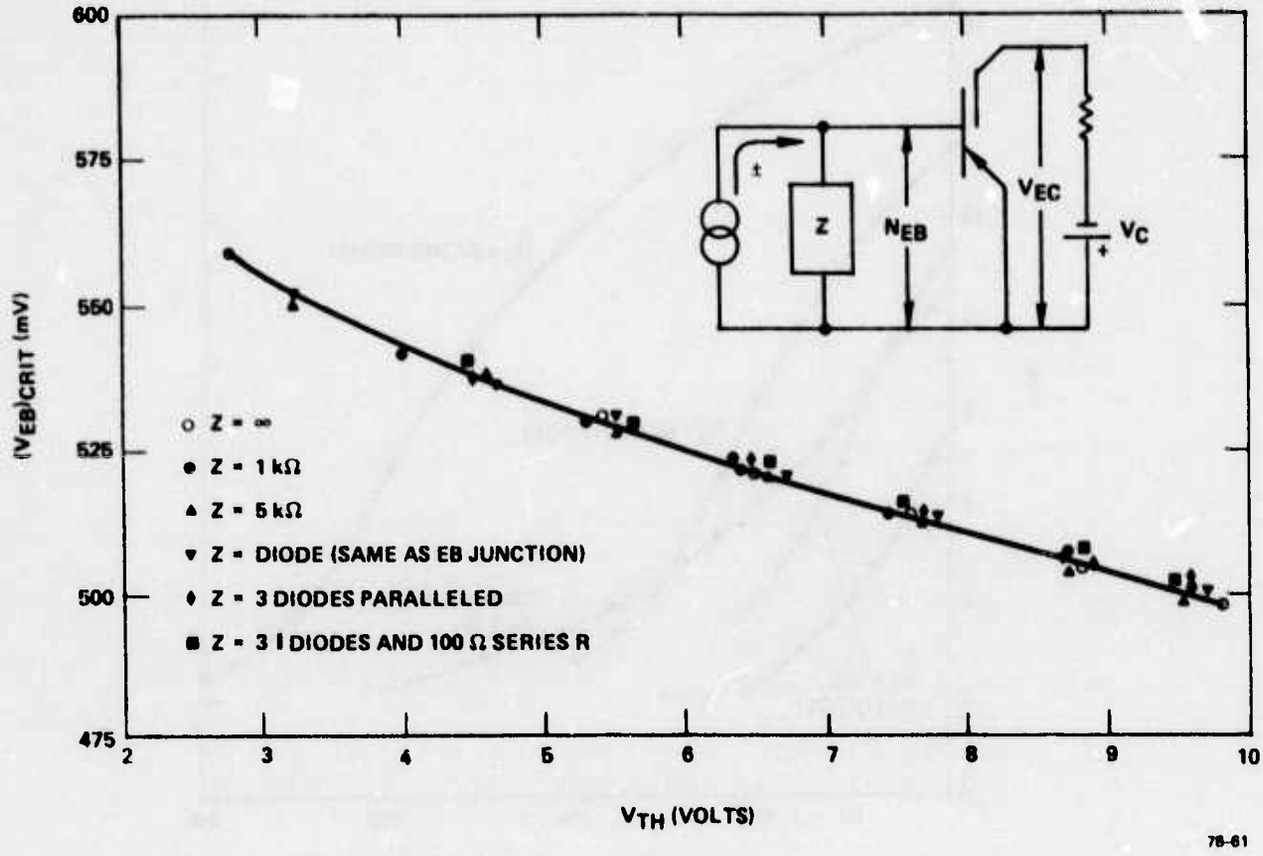

FIG. 13 Critical emitter-base potential when device is biased to $V_{EC} = V_{TH}$ in high impedance state as a function of V_{TH} for various emitter-base shunt impedances.

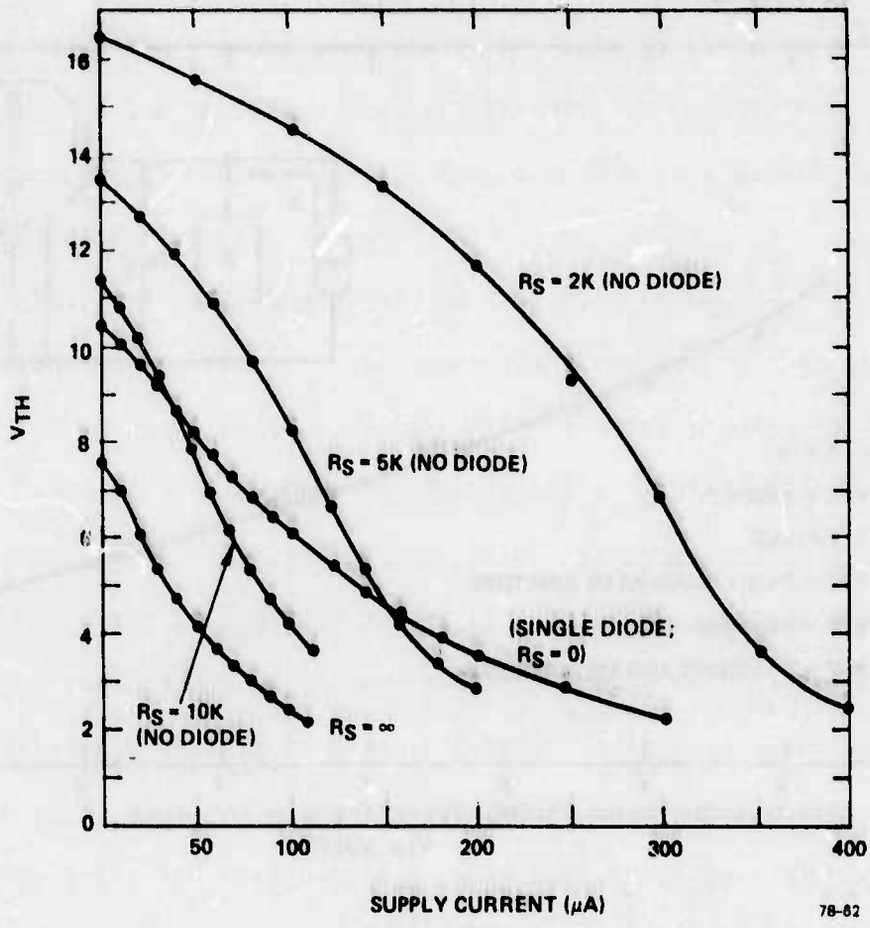

FIG. 14 Threshold voltage V_{TH} as a function of current drawn from base terminal when emitter-base terminals are shunted by various external impedances.

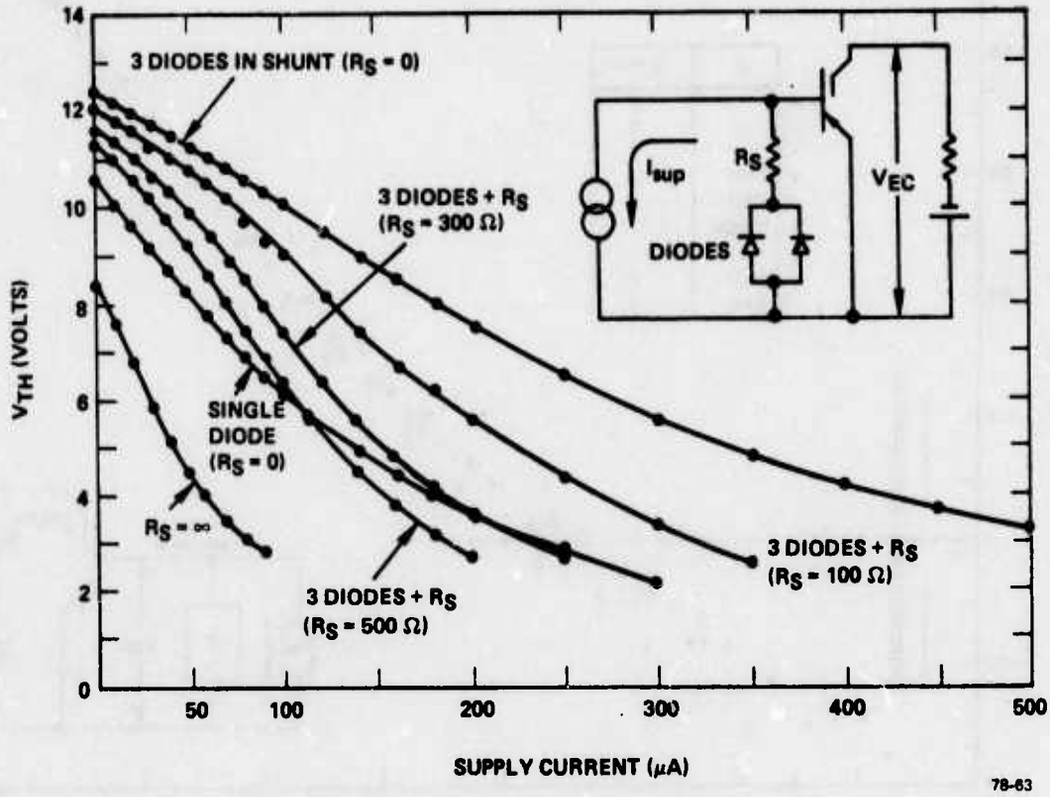

FIG. 15 Threshold voltage V_{TH} as a function of current drawn from base terminal when emitter-base terminals are shunted by various external impedances.

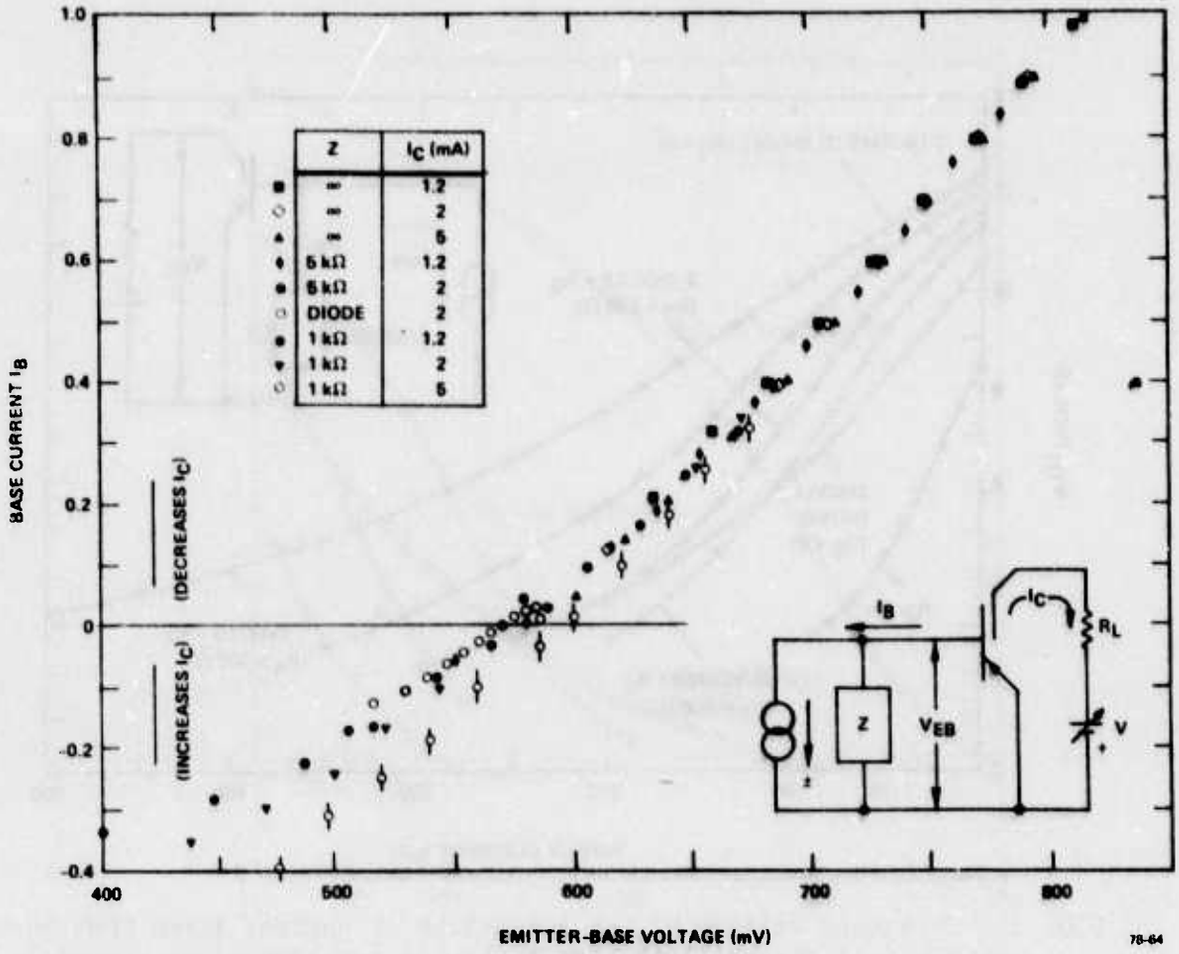

FIG. 16 Base current a function of emitter-collector potential for device in its low impedance state for various values of collector current and emitter-base shunt impedances. Note that base current can enter device at low values of V_{EB}.

values of collector current will cause a larger value of base current to be drawn into the device when the emitter-base voltage is low. At higher values of emitter-base voltage, the base current which is drawn out of the device becomes relatively independent of circuit configuration and collector current.

B. ANALYSIS OF ARRAY WITH DIODE ISOLATION

The above discussion has pointed out the reasons for the interaction between devices within a single base row of the memory array and indicated, so far, one slight advantage for the use of diode isolation. There is a more fundamental reason for preferring the diode isolation rather than the resistance isolation of bases with a memory array row. The array circuit which is the subject of this section is shown in Fig. 17 for a 2 x 2 grounded emitter array.

The most important advantage of this array circuit is readily apparent from examining Fig. 17. No device in its low impedance state can draw current into its base region because this would reverse bias the diode. The fundamental reason for interaction between high-impedance-state devices and low-impedance-state devices with a single row is therefore absolutely prohibited for such a circuit. Experimental operation of such an array circuit confirms that the interaction is absolutely prohibited without requiring a low internal impedance of the base current supply or, equivalently, a shunt diode across each emitter-base row. Another advantage of the array circuit of Fig. 17 compared to the circuit of Fig. 8 is related specifically to the fabrication of integrated circuits. Junction diodes are more easily fabricated than resistors in integrated circuits.

There are two minor disadvantages to the array of Fig. 17 compared to the array of Fig. 8. One is a requirement for higher power to perform

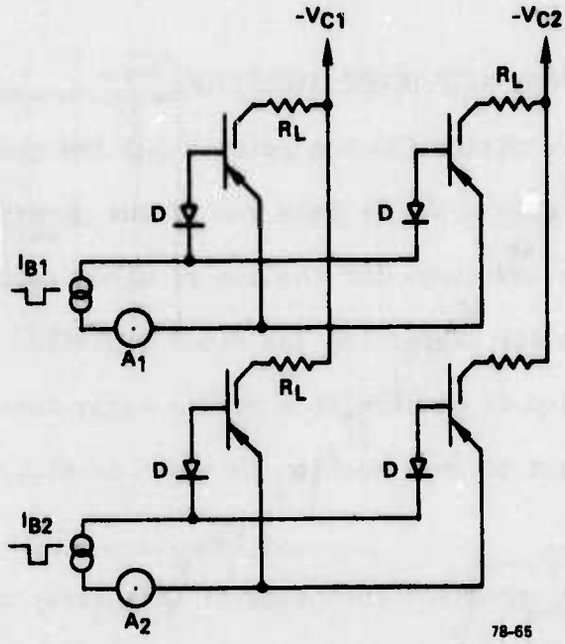

FIG. 17 Memory array with diode isolation between base line and individual base terminals within a row.

the WRITE operation. In order to bring a device into the low impedance state by a double half-select collector column voltage increment and base row current increment, about twice the power must be applied to the base row. This is because the diode D must be brought to a bias of the order of 0.5 V, whereas the voltage drop across the R_{EB} of the circuit of Fig. 8 is only the order of 10^{-2} V. In both cases, of course, the emitter junction must be raised of the order of 0.3 - 0.5 V.

The other disadvantage involves the ERASE operation. The minimum resistance between a base terminal and emitter row cannot be brought to a very low value in order to perform a single element transfer to the high impedance state. The ERASE operation can be performed by other means, however. One possible operation is the erasure of an entire column and the subsequent rewriting of all devices originally in their low impedance state except for the single row in which that device residue which one desires to ERASE. Such operations are conveniently performed in standard memory chips and would permit the circuit to appear functionally identical to the circuit of Fig. 8. Another method of performing the ERASE operation is by applying base current to all but the selected row which has devices in the selected column in their low impedance state and simultaneously lowering the column's collector supply voltage. Although this latter operation does permit a single bit ERASURE, it requires that the information on the selected column be read out and stored so that its advantage over the previous column ERASE and reWRITE is not significant. The circuit of Fig. 17 does permit convenient word (column) operation and for many applications, is, in fact, desirable.

C. DESIGN OF INTEGRATED MEMORY ARRAY

An integrated memory array was designed according to the circuit diagram of Fig. 17. The circuit was designed with the following general considerations:

(1) Since the time and funds available would permit only about six wafers to be processed, no process steps could be included which did not seem simple.

(2) For similar reasons, no fine line design rules would be considered, and

(3) No on-chip decoding and address circuitry would be included since there was no time available to troubleshoot an integrated circuit which could perform these functions.

For these reasons, no attempt was made to use dielectric isolation of devices even though preliminary experiments showed that lower sustaining currents could be obtained if the processing was precisely performed. Thus junction isolation was used throughout. The general circuit design considerations which were followed included:

(1) Buried layer emitter rows. This avoided uncertainties in design of crossover insulators which, however, should ultimately offer much improved performance.

(2) Base row underpassings (under metal collector columns) were produced by n^+ diffusions or implantations.

(3) Collector load resistors were produced over the exact active area of the collector by deposition of amorphous germanium of the required resistivity. While this conserved area on the circuit it did force us to use the least studied of the procedures required for the fabrication.

(4) Molybdenum-gold metallization was exclusively chosen. This permitted a direct transation of the collector metallization used most extensively in discrete devices.

D. FABRICATION OF INTEGRATED ARRAY

The major fabrication problem encountered in the fabrication studies were not related to the ICS device per se, but arose from the lack of availability of clean rooms. Except for photoresist application, all operations including diffusions, evaporations or sputterings, and etchings were not performed in a clean environment.

The second major problem encountered was probably material related but could also have been aggravated by the lack of clean facilities to perform diffusions. This problem was the "spiking" of the nested n^+ diffusion through previously performed p^+ diffusions. The p^+ diffusions were much deeper ($\sim 4\ \mu$) than the depth ($\sim 1\ \mu$) of the n^+ diffusions performed in other starting materials. Both diffusions performed separately on different materials produced junctions with excellent reverse bias characteristics. The "spiking" of the n^+ diffusions ruined isolation of the devices. This was circumvented only by producing the n^+ regions by ion implantation and annealing at temperatures below 830°C. Higher annealing temperatures again caused shorts. This was a major complication to the process, since we did not have time to reorder masks. Only a thin isolation oxide was grown over the n^+ regions, whereas the masks we designed under the assumption that more than 2000 Å of thermal oxide would be grown during the phosphorus drive-in diffusion. Deposited SiO_2 layers were therefore sometimes used in addition to the oxide grown at 830°C.

All yield problems were traced to this spiking or the use of a deposited SiO_2 layer. No failure of the ICS structures themselves were observed in these fabrications.

The major problem anticipated in the fabrication of integrated versions of the ICS was a perimeter dependent current which could greatly increase the sustaining current. The perimeter-dependent current had been observed to be greatly increased if collector metallization covered the edge of the active collector area which was surrounded by a thick insulating oxide. The only reasonable way to prepare the thin ($\approx$ 30 Å) active oxide was to etch away the thicker oxide window and regrow (at 550-700°C) the conducting oxide.

The structure produced by conventional processing and shown in Fig. 18(a) often resulted in high sustaining currents. Removal of the metallizations at the edges of the active collector area produced the structure shown in Fig. 18(b) which had a small sustaining current and which only rarely had a perimeter sensitivity. The structure of Fig. 18(b) is, however, not suitable for integrated circuits.

A device whos cross section is essentially the same as that of Fig. 18(a) was successfully produced by special processing. The important step is to remove the photoresist which patterns the window used to define the active collector by dry oxygen plasma stripping. While this should obviously permit a more uniform removal of the photoresist and therefore a more uniform growth of the thin oxide, the effect of plasma-stripping is more subtle.

Silicon wafers which have only 6-8 Å of nascent oxide on their surface after removal from a buffered HF solution, will emerge from the oxygen plasma with 15-30 Å of oxide. This oxide has been used as the active

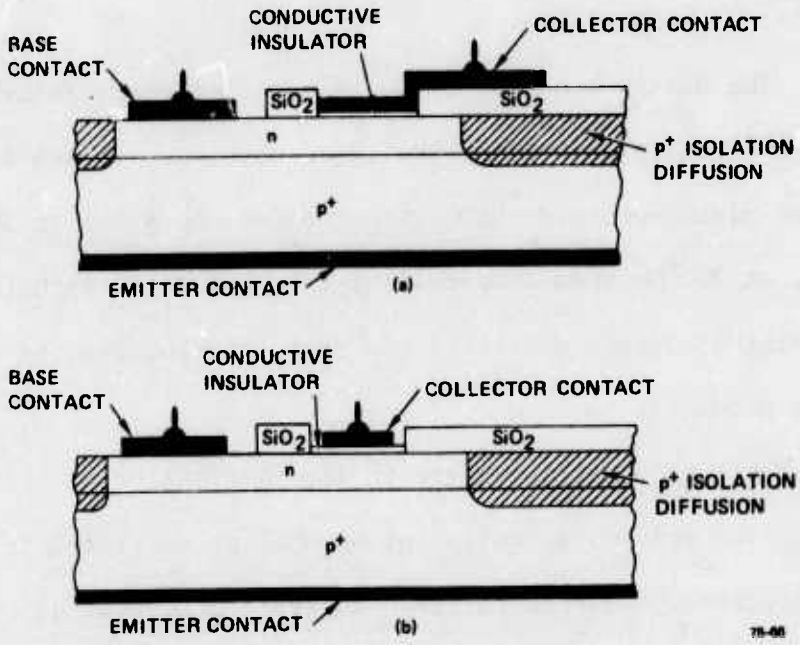

FIG. 18 Cross sectional views of discrete ICS device.

(a) Collector metallization covering window etch. Perimeter-dependent current is commonly observed.

(b) Collector metallization removed from edge of active collector. Perimeter-dependent current not usually observed.

conducting insulator of ICS devices which have very attractive I-V characteristics, including the property of not having perimeter-dependent currents. Unfortunately, the oxide produced by the plasma is not the same from run to run with regard to surface states so that the magnitude of the sustaining current is not predictable.

The plasma-produced oxide is not completely removable in buffered HF. 15-20 Å remain even after prolonged etching. It was found that if this 15-20 Å of plasma-produced SiO_2 was annealed and grown to 30-35 Å thickness in dry O_2 at 700°C, then an excellent thin insulator structure was produced. Low sustaining current densities and perimeter-independent current were consistently produced.

This procedure was used in the fabrication of all the integrated circuits. The procedure, while not unusual or unrelated to other integrated circuit processes, must be followed to avoid difficulties in proceeding with the ICS portions of the integrated array.

E. LAYOUT OF THE INTEGRATED ARRAY

The seven photoresist masks used to produce the integrated array are shown in Fig. 19a-g. Figure 19a is a diagram of the buried emitter rows. The buried layers were grown on an n-type (111) silicon wafer and an 8 μm thick n-type epitaxial layer with doping density equal to 5×10^{15} cm^{-2} was grown on top of the p^+ diffusions produced by masking, using the pattern of Fig. 19a.

Figure 19b is the mask used to pattern a deep boron diffusion which is driven deep enough to contact the buried layer (if the buried layers are underneath this pattern). The function of this diffusion is threefold: (1) Ohmic contact to the buried layers; (2) Isolation of base regions of

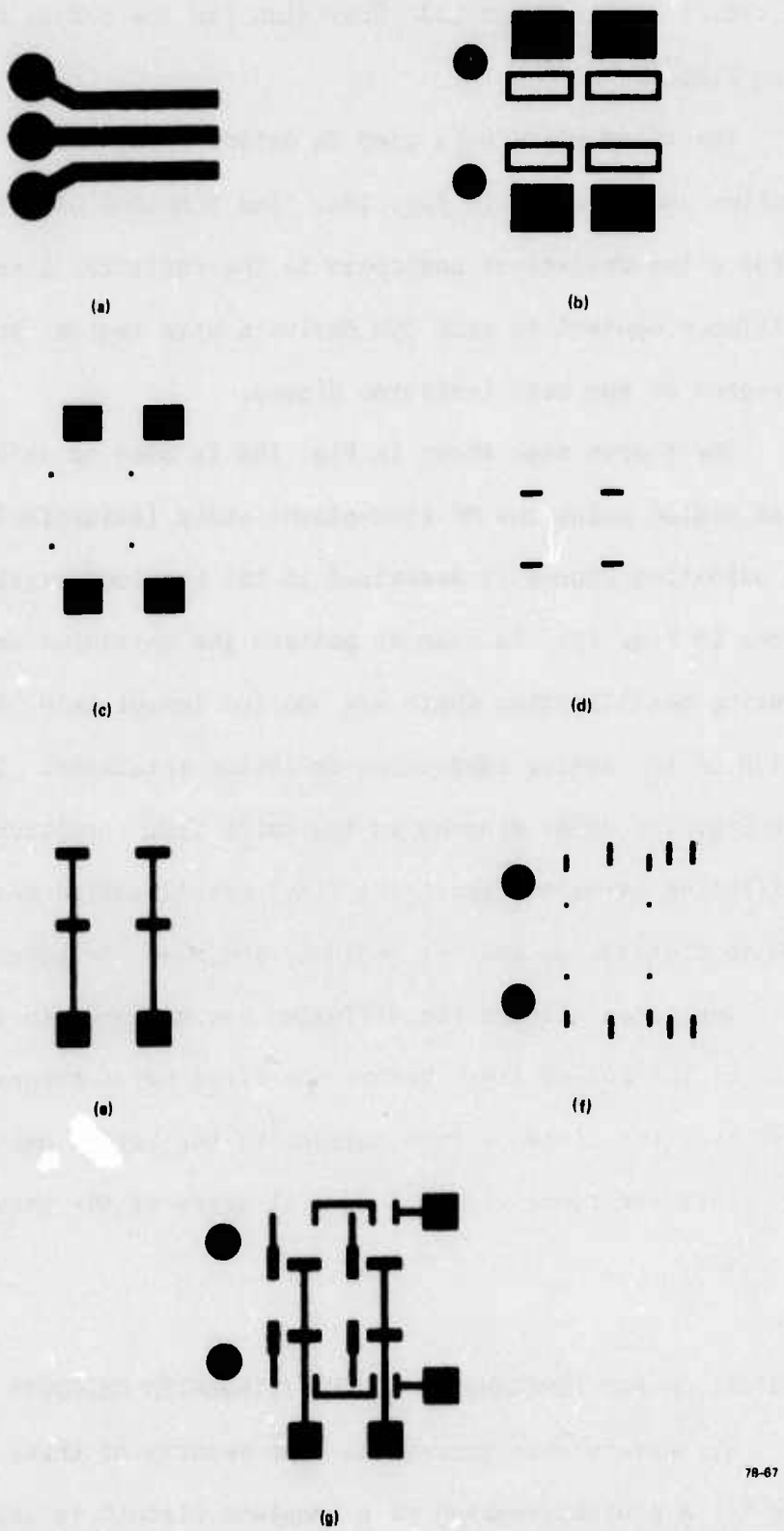

FIG. 19 Photoresist mask patterns used for fabricating 2 x 2 integrated memory array.

(a) Buried p layer; (b) Boron diffusion; (c) Phosphorus diffusion; (d) Active collector definition; (e) Collector metallization and load resistor definition; (f) Contact window definition; (g) Final metallization.

the individual devices; and (3) Provision for the p-type region of the base isolation diodes.

The third pattern is used to define a phosphorus diffusion or implantation and is shown in Fig. 19c. The function of this diffusion is to provide a low resistance underpass to the collector lines, to provide a low resistance contact to each ICS device's base region, and to provide the n-type region of the base isolation diodes.

The fourth mask shown in Fig. 19d is used to define the active collector region using the HF etch-plasma strip (oxidation)-HF etch and thermal oxidation procedure described in the previous section. The fifth mask shown in Fig. 19e is used to pattern the germanium collector resistor and covering metallization which are applied immediately after completing the production of the active conducting collector insulator. The sixth mask shown in Fig. 19f opens windows in the thick SiO_2 insulator grown in previous diffusion steps to permit the final metallization mask patterned by Fig. 19g to contact the emitter regions, and base row interconnections.

The times alloted for diffusion devices and, in some cases, cross diffusion of the buried layer before the first boron predepositions are chosen so that the distance from surface to the buried emitter junction is 2-3 μm. Cross sectional views of several parts of the structure are shown in Fig. 20.

F. FABRICATION AND PERFORMANCE OF THE INTEGRATED CRICUITS

Six wafers were processed: the results of these tests are listed in Table 2. A photomicrograph of a complete circuit is shown in Fig. 21. The circuits of wafer 6 worked as expected. Note that the problems encountered were not due to ICS structure per se, but involved only those

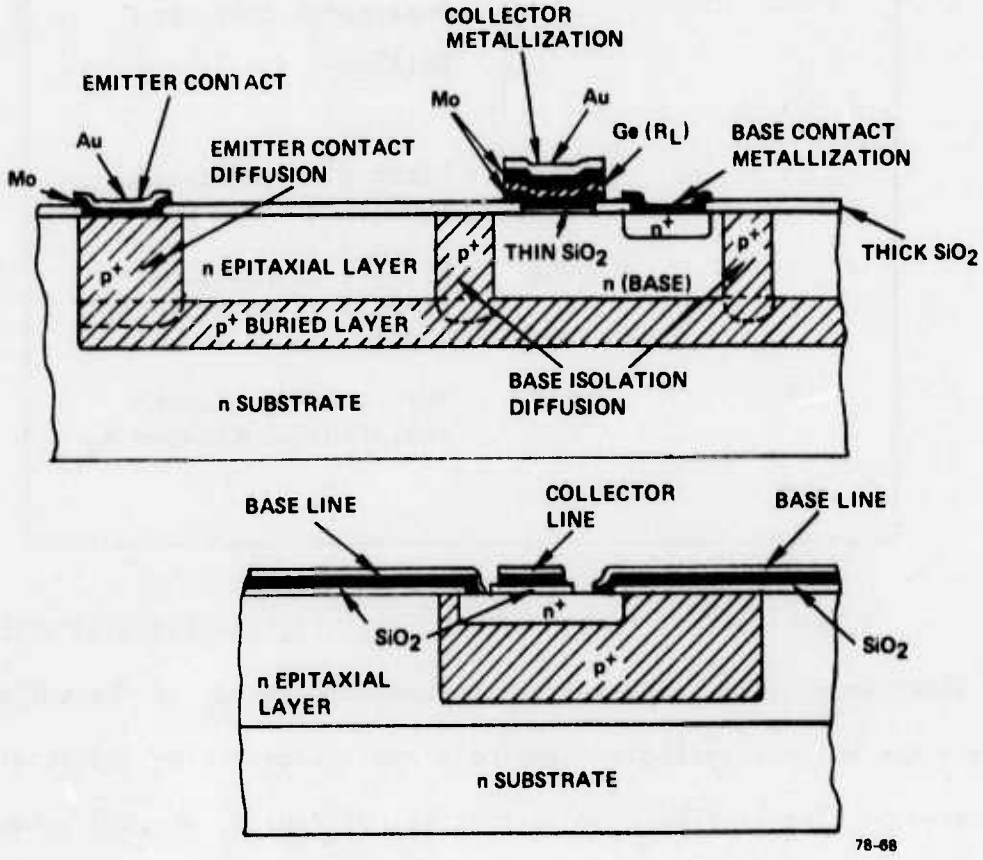

FIG. 20 Cross sectional views of various portions of integrated array.

steps which, if performed in a clean environment with better quality material, could be expected to be performed with extremely high reproducibility.

Table 2.

Wafer Number	Yield	Problem
1	0	Phosphorus diffusion spiking.
2		
3		
4	~ 10%	First n^+ implantation: isolation oxide breakdown.
5	~ 25%	Mistake in photoresist removal of etched metal lines.
5a	~ 10%	Rework of 5; contact resistance increased V_S.
6	~ 100%	-

Typical output characteristics of a single isolated device on the are shown in Fig. 22. The voltage represents the sum of the voltage drop across the emitter-collector terminals and the germanium collector load resistance. The applied base current is, of course, divided between two devices of the array along a row. The sustaining current density is less than 100 μA. If the integrated devices had the same sustaining current density as the discrete devices on which they were modeled, then the sustaining current should have been 25-30 μA. As noted above, complete trouble-shooting of the processing of small area collectors was not worked out before integration fabrication had begun. The higher holding power density requirement was the only way in which the integrated devices fell short of performance expectation.

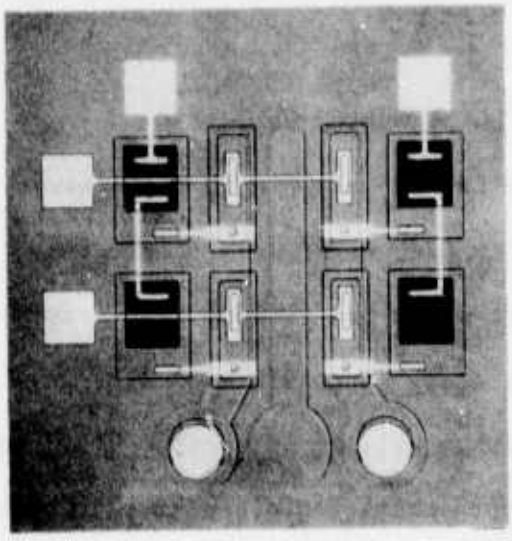

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FIG. 21 Photomicrograph of completed 2 x 2 memory array circuit.

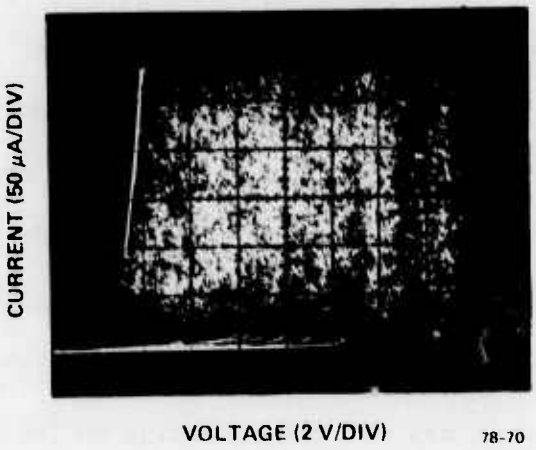

FIG. 22 Output characteristics of integrated device. Voltage is sum of voltage across emitter-collector terminals of the device and germanium collector load resistor. Base current drive (to entire row) is 0, 10, 20, 30, 40 and 50 μA with V_{TH} suppressed to 8 V from 12.4 V.

SECTION 4

PROJECTED PERFORMANCE OF ICS MEMORY ARRAYS

A. LAYOUT OF PROPOSED INTEGRATED CIRCUIT

Although it is not possible to definitively project yields and performance of chips which have never been fabricated, modest extrapolations are possible from the work which has already been accomplished. The projection will be based as completely as possible on experimental results. Thus, for example, a proposed array will be integrated using junction isolation rather than the ultimately more promising dielectric isolation since junction isolation has been used to fabricate the only arrays built to date. The projection will assume that the best performance[1] obtained from discrete devices with regard to sustaining current density and voltage, etc. will also be obtained from integrated devices if time is available to develop the proper processing steps.

The proposed layout of a single memory cell is shown in Fig. 23. For the sake of clarity, the buried p layer which runs below most of the upper p diffusion (including, of course, underneath the active device area) is not shown. This circuit is substantially the same as the already fabricated integrated cells with two major differences. Smaller size is assumed and a two-layer metallization is chosen to reduce resistances of emitter lines and base line underpasses. The layout was derived according to the following rules:

(1) Minimum metal line width: 4 μm.

(2) Minimum spacing on a single mask: 3 μm.

(3) Minimum window dimensions: 4 μm x 4 μm.

(4) Minimum distance between edges of sequentially performed diffusions: 4 μm.

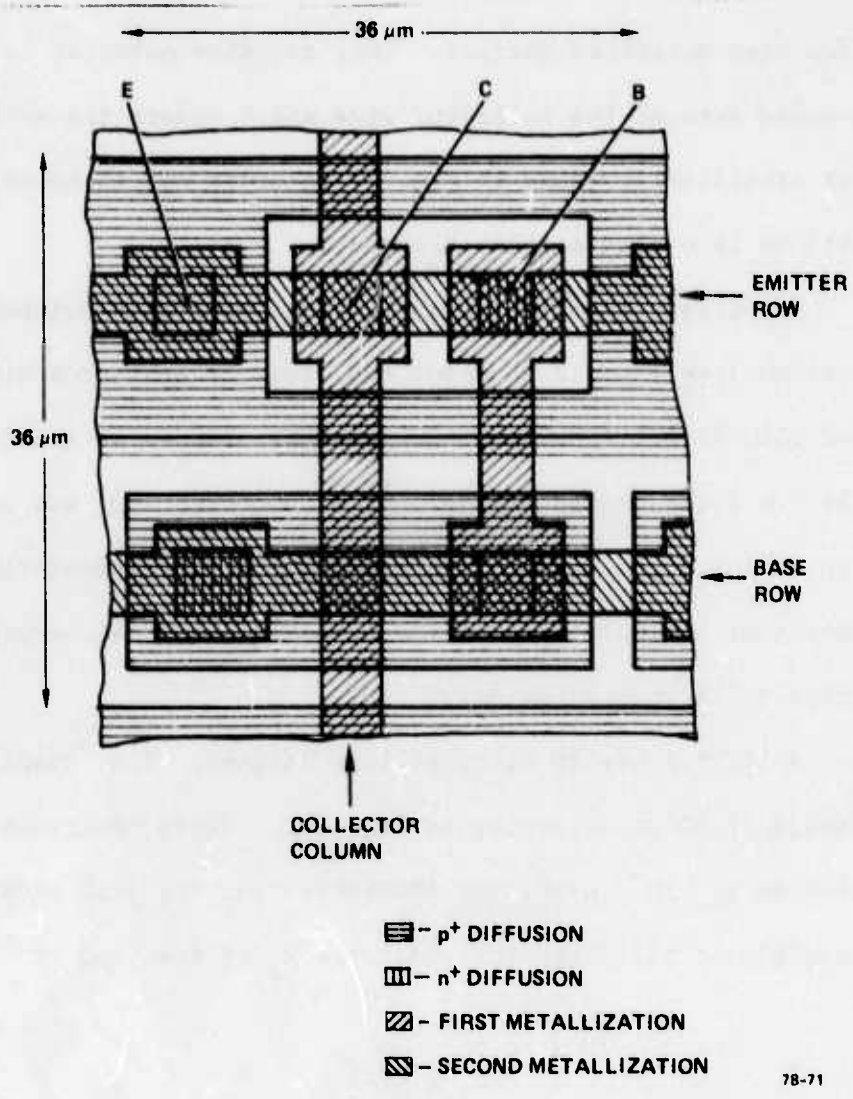

FIG. 23 Layout of proposed small area ICS memory cell.

(5) Alignment error in sequential maskings: $\pm$ 2 μm.

The collector load resistance for each device is assumed to be placed directly over the active collector as was done in the 2 x 2 arrays which have been described earlier. This resistor material is placed under the broadened area of the collector line which covers the active collector. It is not specifically shown in Fig. 23 in order not to cause unnecessary complications in a single color diagram.

The insulator material which might be placed between the two metallization layers could be deposited glass or sputtered SiO_2. Properly sputtered SiO_2 of 0.1 - 0.2 μm thickness has yielded no shorts on two wafers of 2 x 2 integrated arrays. (The sputtered SiO_2 was used in these wafers as an insulator between metal and silicon, necessitated only because of a phosphorus implantation and low temperature anneal, which prohibited growth of a thick thermal oxide.)

A 16K bit memory array will be assumed. The repeat distance between memory cells is 36 μm according to Fig. 23. Taking the resistivity ρ of the metal line to 3×10^{-6} Ω-cm, the thickness t of the line equal to 0.5 μm it is possible to calculate the resitance R_ℓ of the line as

$$R_\ell = \rho \frac{\ell}{wt} \quad , \qquad (1)$$

where ℓ is the required line length which is equal to 128 (3.6×10^{-3})cm = 0.461 cm., and w is the line width = 4 μm. Therefore,

$$R_\ell = \frac{(3 \times 10^{-6})(0.46)}{(4 \times 10^{-4})(5 \times 10^{-5})} = 70\ \Omega \quad .$$

The capacitance C of these lines may be approximated as

$$C_\ell = \frac{(\epsilon_{SiO_2})\, W\ell}{h} \quad , \tag{2}$$

where h is the height of line above the silicon (equal to the thickness of the SiO_2 insulator). Taking $h = 5 \times 10^{-5}$ cm as an average value along the line

$$C_\ell = \frac{(.3 \times 10^{-12}\ \text{F/cm})\ (4 \times 10^{-4}\ \text{cm})\ (.461\ \text{cm})}{(5 \times 10^{-5}\ \text{cm})}$$

or $C_\ell \approx 1$ pF.

B. ARRAY DELAY TIMES

1. Delay Required to Bring Word Line up in Voltage

The resistance and capacitance of the line R_ℓ and C_ℓ are, of course distributed. We assume for simplicity the circuit shown in Fig. 24 is applicable. This circuit requires the full line to be charged before any of the devices are raised in voltage, and therefore represents the worst case for the time interval required to charge any single device. The time required to charge an individual device after the word line has been brought up in voltage will be approximately $R_L C_D$, where R_L is the load resistance and C_D is the device capacitance. The capacitance of an individual device is determined by collector area for both high and low impedance states.

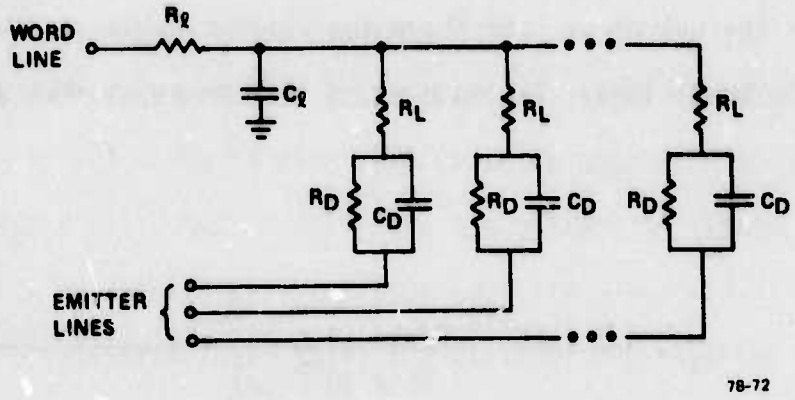

FIG. 24 Apporoximate equivalent circuit diagram of word-line address.

For discrete devices whose area is 1.25×10^{-4} cm^2, the measured capacitances are $C_{D_L} \sim 1.0$ pF and C_{D_L} is less than 5 pF at currents required for holding information in the array and increased to about 10 pF during the read operation. The area of the active collector of the devices of Fig. 23 is 1.6×10^{-9} cm^2. Therefore, we expect

$$C_{D_H} \approx 6.4 \times 10^{-4} \text{ pF}$$

$$C_{D_L} < 1.3 \times 10^{-3} \text{ pF}$$

The time required to charge an individual device after the line has been charged is therefore $R_L C_{D_H} = (120\ \Omega)(10\ \text{pF}) = 1.2$ ns for discrete-array devices. The same product will hold for smaller area devices. This assumes the worst case of $C_D = C_{D_L}$ and, furthermore, that we do not choose to take advantage of "reading" the initially high transient current of a low impedance state device ($C_{D_L}/C_{D_H} \approx 10$, so that the "instantaneous" current which flows after the line has been charged could serve to "read" the device). The time required for the response of the device to represent conduction current as distinguished from displacement current will be given by $R_D C_D \approx (10\ \Omega)(10\ \text{pF}) \approx 0.1$ ns.

The time required to charge an individual device will be less than $R_\ell C_\ell + R_D C_D$, which is 0.17 ns, if the voltage driving source has no internal impedance. If, however, the addressing circuitry is not a perfect voltage source (it has some internal impedance) then the time required to bring an individual device to its final current carrying state can be longer. Let us assume the opposite case, that the address circuit output is a bipolar transistor which acts as a current source.

The current output capability of such a word address amplifier will be chosen to be equal to a bipolar transistor whose collector area is $\approx 10^{-4}$ cm^2, which is a much larger area than the individual devices but not as a worst case. We assume that the address circuit must charge the total capacitance of the line which is denoted by C_T. We also define the following symbols as

N_L = number of devices in line in low impedance state

N_H = number of devices in line in high impedance state

$N = N_L + N_H = 128$

It follows that

$$C_T = C_\ell + N_H C_{D_H} + N_L C_{D_H} \tag{4}$$

For the worst case ($N_L = N$),

$$C_T \approx [1 + (128)(1.3 \times 10^{-3})] \text{ pF}$$

or

$$C_T \approx 2.6 \text{ pF} \quad .$$

The address driver with the assumed area can easily deliver 1 mA of current. The time required Δt to raise the potential of a device by 0.1 V (a typical value used in the discrete array and in the 2 x 2 integrated arrays) will be therefore given by

$$\Delta t = \frac{C_I(0.5)}{I} \tag{5}$$

where I is the maximum current which can be supplied by the address driver.

Taking I = 1 mA, as shown previously,

$$\Delta t = \frac{(2.6 \times 10^{-12})(0.1)}{10^{-3}} = 0.26 \text{ ns}$$

which is a comfortably small time interval.

2. Total Read Access Time

The total read access time τ_A is given by

$$\tau_A = \tau_{decoder} + \tau_{drive} + \Delta t + \tau_S$$

where Δt = time required to raise an individual device's voltage as calculated above and τ_S is the time required to turn on a sense amplifier.

We estimate τ_S by assuming that the sense amplifier is a bipolar transistor formed along with the ICS devices in the same processing. The major contribution to τ_S is expected to be the base capacitance C_B which must be charged through the output line R_ℓ. We estimate that $C_D < 10$ pF, therefore we take $\tau_S < (70\ \Omega)(10\ \text{pF}) = 0.7$ ns.

We therefore have

$$\tau_A < \tau_{decoder} + \tau_{drive} + 1 \text{ ns} + 0.7 \text{ ns} \quad .$$

We expect $\tau_{decoder} + \tau_{drive}$ to be comparable to that obtained in bipolar circuits and, therefore,

$$\tau_A \approx 20\text{-}50 \text{ ns} \quad .$$

C. POWER REQUIREMENTS OF THE ARRAY

1. Holding Power

The power P required to pass a current I_C through a device in the array of Fig. 23 is given by

$$P = I_C V_C + I_C^2 R_L \tag{6}$$

where V_C is the emitter-collector voltage. For values of $I_C \leq 5\ I_S$ (where I_S is the sustaining current), $V_C \approx V_S$ (where V_S is the sustaining voltage). In practice, I_C has been chosen to be approximately $3I_S$ for convenient operation. Therefore, the minimum power we chose to supply to the device is

$$P \approx I_S V_S + 9 I_S^2 R_L \quad . \tag{7}$$

The minimum current density observed for discrete devices with the SiO_2 insulator is 1.6 A/cm^2, with 2 A/cm^2 being more reproducible. For a device as in the array of Fig. 23, I_s = 0.32 μA, with V_S = 2 V and $R_L = 10^4\ \Omega$,

$$P = (0.32)\ 10^{-6}(2) + 9\ (0.32)^2\ (10^{-6})^2\ 10^4 \tag{8}$$

or

$$P \approx 6.4 \times 10^{-7} + 9 \times 10^{-9} \approx 0.64\ \mu W \quad .$$

The power required to hold 16K bits in the "1" state is therefore of the order of 10 mW.

2. Power Required to Perform Operations on Array

(a) Read operation. In order to read a word, a current density of about twice the holding current is required to unambiguously perform

the operation in discrete array. The extra power P_R required to perform a read operation on a single device is, from Eqs. (6) and (7)

$$\begin{aligned} P_R &\approx I_C V_C + I_C^2 R_L - (I_S V_S + 9 I_S^2 R_L) \\ &\approx 2I_S(V_S + V_S/4) + 9(2I_S)^2 R_L - (I_S V_S + 9 I_S^2 R_L) \\ &= (1.5) I_S V_S + 27\ I_S^2 R_L \\ &= (1.5)(0.32\ \mu A)\ 2\ V + 2(0.32\ \mu A)^2\ 10^4\ \Omega \\ &= 9.6 \times 10^{-7}\ W + 2 \times 10^{-9} \approx 0.96\ \mu W \end{aligned} \tag{9}$$

The maximum extra power for an entire "word" of 128 bits is therefore $\approx$ 125 μW. This is much less than the power required to hold information in the array (10 mW).

(b) Write operation. The extra power required to write a single bit consists of the power required to supply current to a single base row plus the power required to raise a collector column's voltage P_c ,

$$P_{row} = 2 I_B V_{EB}$$

where V_{EB} is the emitter-base voltage of a single device and I_B is the applied base current. The factor of two obtains because this current must also be applied to each base isolation diode which we assume has approximately the same emitter area as the active devices. Useful values of I_S for the small area devices of the array of Fig. 23 will be of the order of

$$(50 \times 10^{-6}) \frac{1.6 \times 10^{-7}}{1.25 \times 10^{-4}} = 6.4 \times 10^{-8} A$$

since the applied base current required for the proposed array devices should be smaller than that required for the discrete devices by the ratio of their areas. With $V_{EB} \approx 0.55$ V

$$P_R \approx 0.67 \mu W \quad .$$

On the other hand, from Eq. (7)

$$P_c \approx V_c I_c - 3V_S I_S + I_C^2 R_L - 9I_S^2 R_L$$

if the device is in its low impedance state. Therefore, for the worst case when the device is already in its low impedance state

$$P_c = 1 \mu W$$

following similar considerations which lead to Eq. (9).

The total power required to write a word must be less than (128) $(P_c + P_{row}) \approx 128 \mu W$ which is again small compared to the total array holding power of 10 mW.

(c) Erase operation. The power required to erase an entire word is actually less than that required to hold information, since the voltage and current supplied to that column is lowered.

D. SUMMARY OF EXPECTED PERFORMANCE

The following table summarizes the expected performance of an ICS array with an approximate comparison with the performance and characteristics of conventional MOS and bipolar random-access memories.

	ICS	MOS	Bipolar
No. bits	16K	16K	256
Static	Yes	No	Yes
NDRO	Yes	No	Yes
Active devices/bit	1	1	4-6
Area/bit	~ 2 mil^2	~ 1 mil^2	75 mil^2
Chip size	4×10^4 mil^2	4×10^4 mil^2	4×10^4 mil^2
Average power/bit (holding)	1 μW	2 μW	1 - 10 mW
Standby power on array	10 mW	35 mW	400 mW
Peak power on array	20 mW	35-50 mW	$\geq$ 400 mW
Total power consumed by chip	210 m	600 mW	400-800 mW
Access time	20 ns	200 ns	20-50 ns

We therefore conclude that the ICS could have lower power consumption an MOS memory chip, and faster access time than a bipolar chip (for the same number of bits).

SECTION 5

NONLATCHING CIRCUITS

ICS devices can be used in nonlatching circuits (circuits which will not remain in the low impedance state when a base or emitter current pulse is removed) by making use of the effect of an emitter-base shunt resistance upon the value of sustaining current and sustaining voltage. The circuit of Fig. 6 is the simplest circuit which contains all the essential features of nonlatching operation. (The switch S must be closed and a base current pulse supplied.) For nonlatching switching it is essential that $R_S \neq \infty$ and that the pulsed supply current which is drawn from the parallel combination of R_S and the base-emitter terminals of the device result in a collector current which is less than $I_S(R_S)$. The common emitter collector output characteristics of Fig. 25 illustrate the desired relationships.

A device originally residing in the high impedance state at point B on the collector characteristics of Fig. 25 can be transferred to a pseudo low impedance state near point A on the low impedance state characteristic that would exist if R_S were much larger than the value actually chosen. It is important for nonlatching operation that point A corresponds to a current less than $I_S(R_S)$. Removal of the base current supply pulse will cause the device to revert to its low impedance state at point B because point A does not lie on a stable impedance state of the device with the particular value of R_S chosen. Clearly, R_S, R_L and V^- must be chosen together correctly in order to obtain the desired behavior.

The nonlatching nature of certain ICS circuits suggests their use in logic applications. An inverter circuit, as diagrammed in Fig. 26 has been operated. The two ICS transistors T_1 and T_2 are essentially identical.

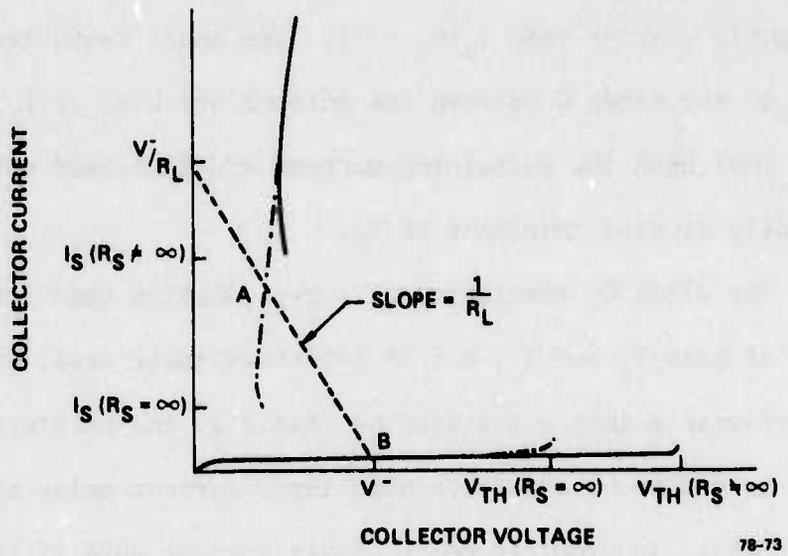

FIG. 25 I-V characteristics of ICS transistor illustrating requirements for nonlatching operation.

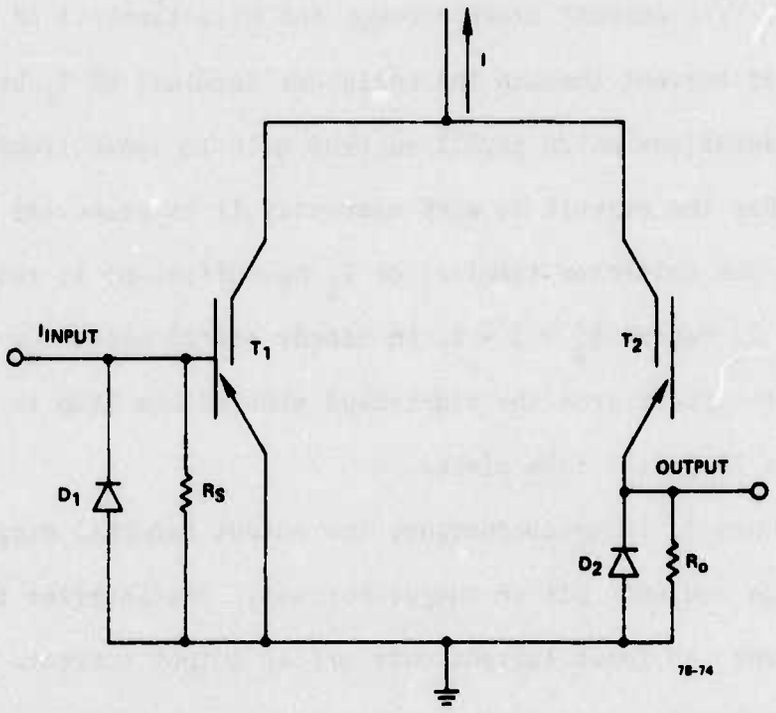

FIG. 26 Diagram of ICS inverter circuit.

In the quiescent state of the circuit T_1 is not conducting and T_2 is conducting, drawing essentially all the collector supply current I. (I is chosen to be slightly greater than $I_S (R_S \approx \infty)$. The shunt conductance consisting of either R_S or the diode D between the emitter and base of T_1 is chosen large enough so that both the sustaining current and threshold voltage of T_1 are significantly greater than that of T_2.

The diode D, consisting of a p-n junction identical to the emitter junctions of both T_1 and T_2, but of 3-5 times their area, was found to give better performance than a resistor by itself as the emitter-base shunt element. T_1 can be turned on by a sufficiently large current pulse supplied to the input terminal. In order to obtain logic current gain it is important that the shunt conductance between the emitter and base terminals of T_1 not be too large or else an extremely large value of input current will be required to turn T_1 on. The current drawn through the base terminal of T_1 can show up as an increased current through the collector terminal of T_1 because of the same considerations which permit current gain in conventional bipolar transistors. For the circuit to work correctly it is essential that the current I_1 leaving the collector terminal of T_1 be sufficient to reduce the current I_2 through T_2 (where $I_2 = I - I_1$ in steady state) below I_S. Then a complete transfer of current from the right-hand side of the loop to the left-hand side of the loop will take place.

When T_2 is nonconducting, the output terminal drops to essentially zero voltage and cuts off an output current. The inverter function is thus accomplished: an input current cuts off an output current. Removal of the input current will cause T_1 to revert to its high impedance state and T_2 will again conduct.

Performance of the circuit demands a stiff current source I, or else only incomplete transfer of the current from one side of the loop to

the other will take place. The speed of transition for the actual operated circuits was about 10 ns. The time internal τ required to make the transition was apparently greatly increased by parasitic capacitances in the breadboard circuit used with discrete devices. A major contribution to τ was the time t_c required to charge D and the emitter junction of T_1. The transistors T_1 and T_2 had emitter areas ten times the area of their collectors so most of the emitter capacitance that was present in the actual circuits could be eliminated. The swing in base voltage required to turn on T_1 is of the order of 0.1 V (change from 0.4 to 0.5 V) and the emitter capacitance was of the order of 100 pF when the device was turned on. Thus, if a current of about 1 mA is drawn from the base of T_1, we expect

$$\tau_c \approx C/I(\Delta V) = \frac{(10^{-10}\ \text{F})(10^{-1}\ \text{V})}{(10^{-3}\ \text{A})} = 10^{-8}\ \text{s} \quad ,$$

as observed.

SECTION 6

CAPACITANCE STUDIES OF ICS DEVICES

A. CAPACITANCE MEASUREMENTS (HIGH IMPEDANCE STATE)

1. Collector-Emitter Capacitance

In order to study the detailed behavior of ICS devices and relate this to the basic physical mechanisms responsible for the ICS phenomenon, the capacitance-voltage characteristics of the devices were studied. From such measurements one generally expects to learn such things as depletion layer width, extent of inversions, etc., which are certainly important in describing device properties. Since different insulator materials will have different conduction mechanisms and therefore, in general, different strengths of inversion not all devices could be studied in detail. This section therefore emphasizes the behavior of one particular device variation, the Mo-SiO_2-n-p^+ structure, for two reasons. First, this device was chosen for integrated circuit fabrication, and, second, the conduction properties of SiO_2 thin insulators have been of interest in other unrelated work including the description of metal-insulator-semiconductor, "Schottky-barriers," and as solar cells or photon detectors.

Figure 27 presents the basic observation on capacitance measurements of ICS devices when terminal connections are made to the emitter and collector. The measurements which were made on a Boonton model 72-DB capacitance bridge at 1 MHz were terminated at the greatest bias at which reliable data were obtained. (Generally a device quality factor $Q = \omega CR$, equal to or greater than unity enabled the bridge to function reproducibly.) The data of Fig. 27 were not extended beyond the point where the device $Q < 2$. Lower frequency measurements were not useful since the conduction

of the device would limit accuracy over most of the range of applied voltages.

A second important point to note is that the experimental data were affected by illumination of the device. This observation is not unexpected. It has been noted that device threshold voltage depends upon illumination. The data suggest that a tendency to invert is obtained at higher biases when the device is illuminated. At low biases the light obviously causes the surface to be accumulated. This interpretation is confirmed by the current-voltage characteristics shown in Fig. 28 for the same device under the identical conditions of illumination. The interpretation of these is complicated by the fact that the apparatus measures the series combination of the capacitance of the emitter junction and the surface.

2. Collector-Base Capacitance

Measurement of the collector-base capacitance of the device avoids the complication of the emitter-junction capacitance. Use of this technique allows the direct confirmation of the fact that there is essentially no inversion obtained in the high impedance state. Figure 29 displays the measured values of $1/C^2$ as a function of the applied voltage for two related structures; a Mo-SiO_2-n-p^+ ICS device and a Cr-n-p^+ Schottky-barrier device made on a wafer from the same lot as the ICS structure. Contact to the n regions of both devices was made by an n^+ phosphorus diffusion; the geometry and heat treatments of both wafers was identical. A chromium Schottky barrier was chosen because chromium is especially active in consuming any oxide layer on silicon.

The linear slope of $1/C^2$ vs applied voltage obtained for both devices implies that there was uniform doping in the epitaxial layer with essentially no inversion. The difference in slopes (which are inversely proportioned to ionized donor density) are within the expected variation for the starting material.

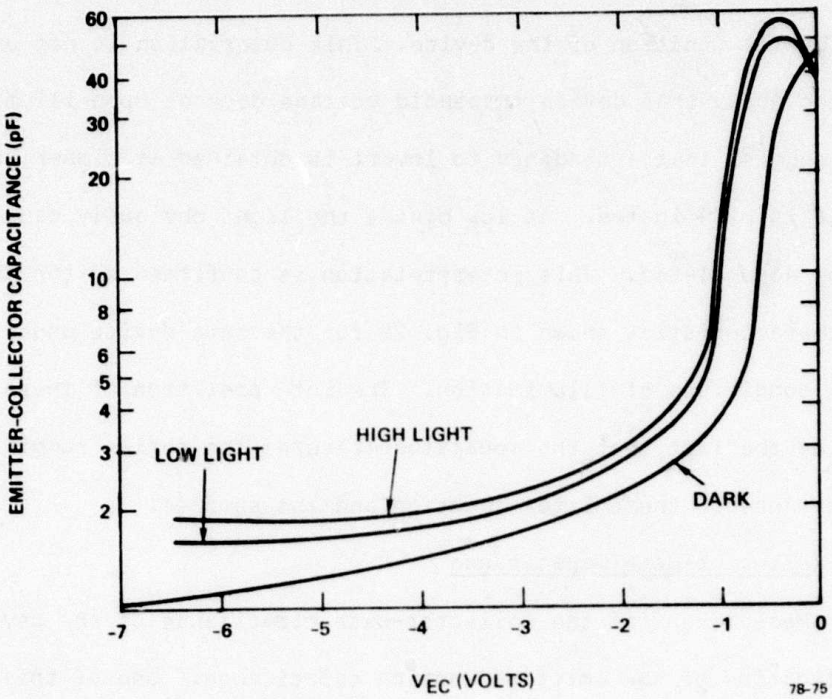

FIG. 27 Capacitance-voltage characteristics of Mo-SiO_2-n-p^+ ICS device. Capacitance is measured across emitter and collector terminals with base terminal open.

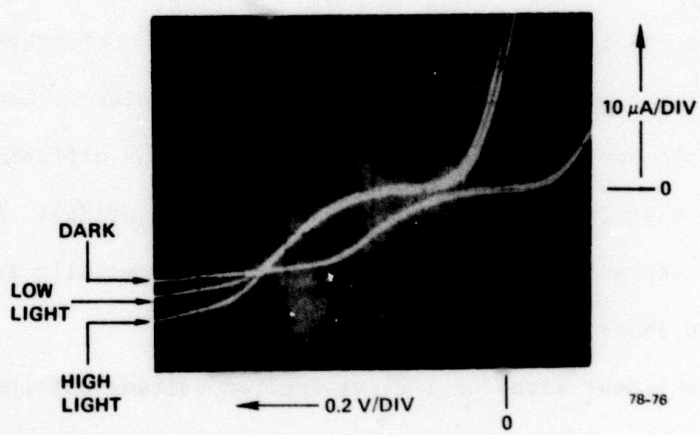

FIG. 28 Emitter-collector I-V characteristics of same device used to obtain data of Fig. 26 with identical conditions of illumination.

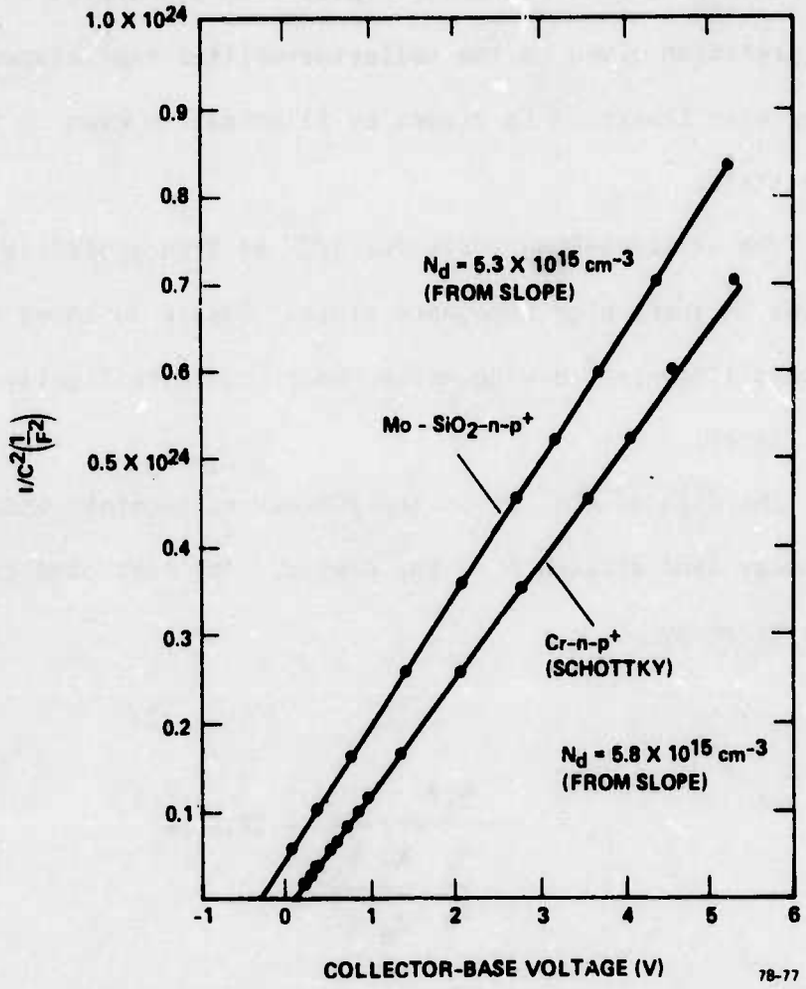

FIG. 29 $1/C^2$ vs applied voltage for Mo-SiO_2-n-p^+ ICS device and a companion Cr-n-p^+ Schottky-barrier device. Terminal connections are made to collector and base with emitter terminal open.

It is important to note that the data for the ICS was obtained with no illumination. Even though the surface of the wafer was largely covered by opaque metal, weak room light illumination was sufficient to cause the $1/C^2$ vs V curve of the ICS to radically depart from linearity, thus confirming the interpretation given to the collector-emitter capacitance data that partial or weak inversion is caused by illumination even in the high impedance state.

The straight-line curve for $1/C^2$ vs V is generally obtained for all ICS devices in their high impedance state. Figure 30 shows a curve obtained on a M-polysilicon-p-n^+ device which had a much more lightly doped and thicker epitaxial layer.

The data of Fig. 29 on the ICS device together enable a determination of the energy band structure of the device. The flat band capacitance of the device is given by

$$C_{FB} = \frac{\epsilon_i A}{d + \frac{\epsilon_i}{\epsilon_s} \frac{kT \epsilon_s}{N_d q^2}} = 18.8 \text{ pF}$$

where A is the device area, d is the thickness of the SiO_2, ϵ_s and ϵ_i are the dielectric constants of the silicon and SiO_2, respectively; k is Boltzmann's constant, T is the temperature in degrees Kelvin, N_d is the ionized donor density and q is the electronic charge. From the data on which the curve of Fig. 29 was based, the flat band voltage is - 0.16 V. Figure 31 presents the surface energy band structure under one assumption that the band structure of the thin SiO_2 layer is the same as that for thick SiO_2 layers. As shown in Fig. 30, the conduction band of the silicon is

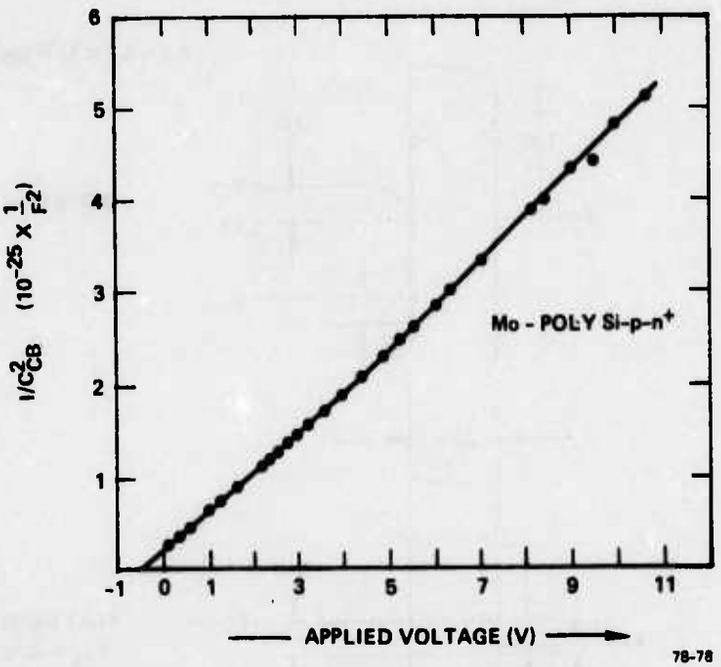

FIG. 30 $1/C^2$ vs applied voltage for a Mo-poly Si-p-n^+ ICS device. Terminal connections are made to collector and base.

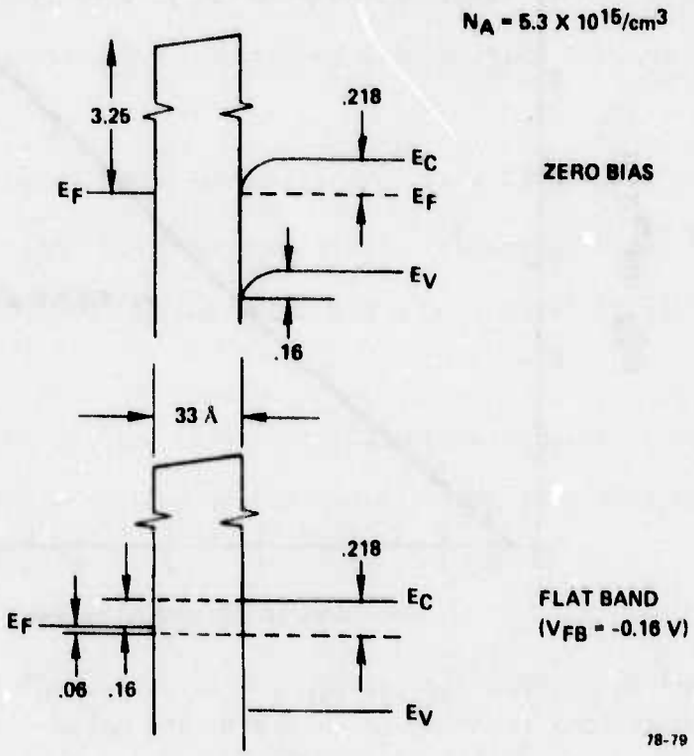

FIG. 31 Energy band diagram of Mo-SiO_2-n-p^+ device at surface. Uniform properties of thick SiO_2 layers are assumed.

aligned with the Fermi level of the metal at an applied bias of 15.5 V. It is at nearly this bias that the threshold of the device is reached, suggesting that electron tunnel current must be present to cause a transition to the low impedance state.

3. Collector-Base Capacitance With Applied Emitter Current

Measurement of the collector-base capacitance of ICS devices is possible when emitter current is applied. (It is not possible to reliably measure the emitter-collector capacitance when terminal is connected to the base because it is not possible to consistently null out the capacitance introduced by the additional circuit.) The results of such measurements are shown in Fig. 32. Note that the capacitance increases with emitter current but that the rate of increase at higher emitter currents is lower.

This behavior suggests that an inversion layer is formed by the action of the emitter current but a detailed quantitative explanation is not immediately obtained. For example, when $I_E = 0$, $C_{CB} = 1.7$ pF at $V_{CB} = 3.3$ V, whereas when $I_E = 100\ \mu A$, $C_{CB} = 1.7$ pF when V = 9.0 V. It is clear that interpreting equal capacitances as equal depletion widths results in contradiction. Such an assumption would require that (for the above example) 4.7 V be dropped across the insulator and the inversion layer. The voltage drop across the inversion layer can be a significant fraction of the voltage drop across the insulator simply because the insulator is so thin (30-35 Å) and the inversion layer could even be thicker (80-100 Å). If the assumption is made that 1/2 of this extra voltage appears across the insulator, then this would require an electric field of the order of 10^7 V/cm across the SiO_2. While the best SiO_2 layers may have dielectric breakdown strengths even greater than this, we have not observed dielectric breakdown strengths above $2\text{-}5 \times 10^6$ V/cm for these materials which were not grown in a clean environment. It should be especially noted that all devices tested would

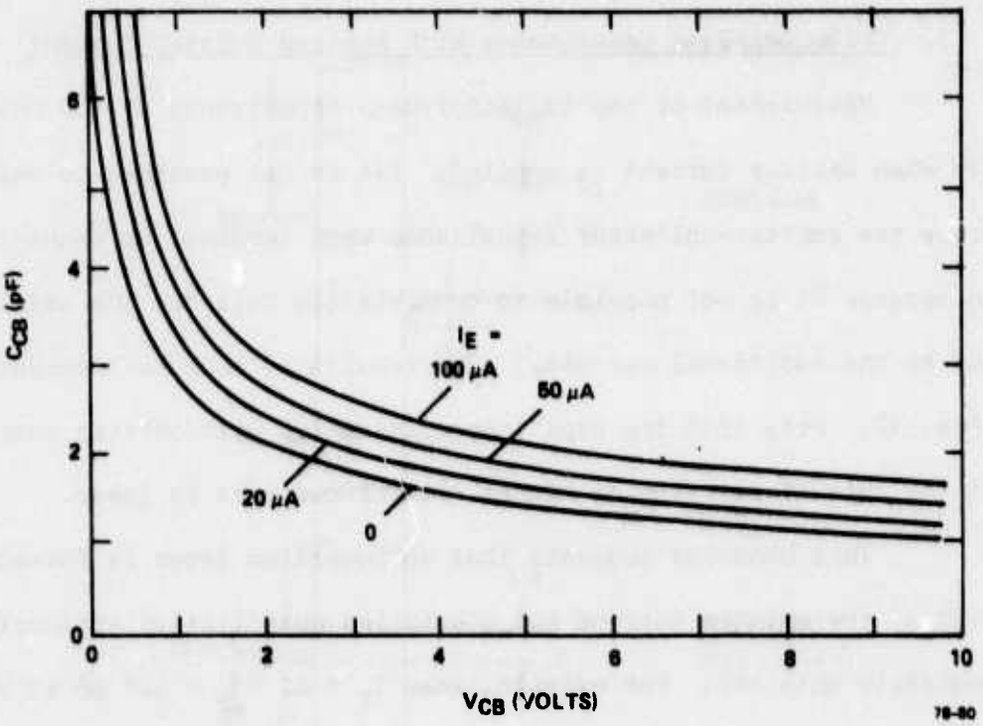

FIG. 32 Capacitance as a function of voltage for collector-base terminals of Mo-SiO_2-n-p^+ ICS device. Emitter current is varied in different traces.

withstand such collector-base voltages and emitter currents and therefore the data of Fig. 32 do not represent an extraordinary case.

The cause of the increased capacitance when emitter current is applied can therefore not be due to decreased depletion layer width because this would imply that the electric field across the insulator would be unreasonably large. Another possible explanation for the increased capacitance which could be considered is conventional diffusion capacitance associated with bipolar transistors. Such an explanation can also be shown to be insufficient.

The diffusion capacitance for grounded base is given by

$$C_{df} = \frac{W_N}{D_p} I_{EC} \left| \frac{dW_B}{dV_{CB}} \right|$$

where D_p is the diffusion constant of holes in the base region, W_N is the width of the neutral base region as defined in Fig. 1 and I_{EC} is the applied emitter current which crosses the collector depletion zone. If N_d is the ionized donor concentration in the base, then

$$\frac{dW_N}{dV_{CB}} = - \left(\frac{\epsilon}{2qN_D}\right)^{\frac{1}{2}} V_{CB}^{-\frac{1}{2}}$$

Taking $D_p = 12\ cm^2/s$, and $N_D = 5.3 \times 10^{15}\ cm^{-3}$ the value of C_{df} at $I_{EC} = 10^{-4}$ A and $V_{CB} = 5$ V is 0.04 pF if $W_B \approx 2\ \mu m$. This value of C_{df} is small

compared to any value of $C_{CB}(I_E) - C_{CB}(0)$, observed in Fig. 31. The small value of C_{df} is not unexpected since the total width between collector insulator and the emitter junction is small ($\approx 4\ \mu m$) compared to the total base widths of transistor structures which have larger diffusion capacitances. It should also be noted that the assumed emitter current received by the collector of 100 μA is much larger than that collected in the actual capacitance experiment because of the small ratio of collector-to-emitter area. The current assumed in calculating the diffusion capacitance is therefore much larger than actually present in the experiments of Fig. 32.

The change in capacitance brought about by the introduction of emitter current must therefore be explained by some other mechanism. A mechanism which can explain this behavior is the capacitance associated with the annihilation of incipient inversion layer change due to the finite conductivity of the insulator and will be described in the next section.

B. THEORY OF COLLECTOR-BASE CAPACITANCE OF THE ICS WITH VARIATION OF EMITTER CURRENT BIAS

The collector-base capacitance C_{CB} of the ICS will be calculated for the device when it resides in its high impedance state under the assumption that the hole tunnel current density J_{pt} is given by

$$J_{pt} = \frac{4\pi m_t e(kT)^2}{h^3} \exp(-\eta) \frac{p_s}{N_v} \qquad (1)$$

where m_t is the transverse hole mass, e is the electronic charge, h is Planck's constant, p_s is the hole concentration at the semiconductor surface, N_v is the density of states in the valence band and $\eta \approx - \chi^{\frac{1}{2}} d$, where χ is

the tunneling barrier height for holes, and d is the thickness of the insulator. Equation (1) has been derived by Card and Rhoderick[1] and by Green and Shewchun,[2] and used to discuss the conduction of holes through thin SiO_2 layers grown on silicon. Based on a two-band model of the band structure of SiO_2, Habib and Simmons[3] evaluate η as equal to 0.936 d, where d is the insulator thickness measured in angstrom units. An implicit assumption involving the use of Eq. (1) is that the localization of carriers in an inversion layer will not substantially affect the tunnel current, which situation has been discussed by Weinberg[4] for tunneling into the SiO_2 conduction band under the action of stronger electric fields than considered here.

In the high impedance state any inversion layer which exists at the semiconductor surface cannot screen the interior of the semiconductor from additional charge which may appear on the collector electrode by the same electrostatic mechanism which applies to a perfect insulating SiO_2 when a low frequency test signal is applied. The unscreening inversion layer of an ICS can, nevertheless, profoundly affect the collector-base capacitance C_{CB} under certain circumstances. The mechanism of this interaction can be explained by referring to Fig. 33, which displays charge density as a function of position near the surface of the device. If only a dc voltage is applied to the collector, then a steady-state inversion charge density Q_{io} at the semiconductor surface and a steady-state width of the surface depletion zone W_o will exist. Increasing the charge on the collector from $-Q_m$ to $-(Q_m + \Delta q_m)$ will <u>not</u> result in an increase of the width of the depletion layer from W_o to $W_o + \Delta q_m/eN_d$, however (here N_d is the density of ionized donors near the semiconductor surface). This smaller increase in depletion width results from an increase in hole tunnel current caused, according to Eq. (1), by an increase in p_s. Thus, a portion of the increment

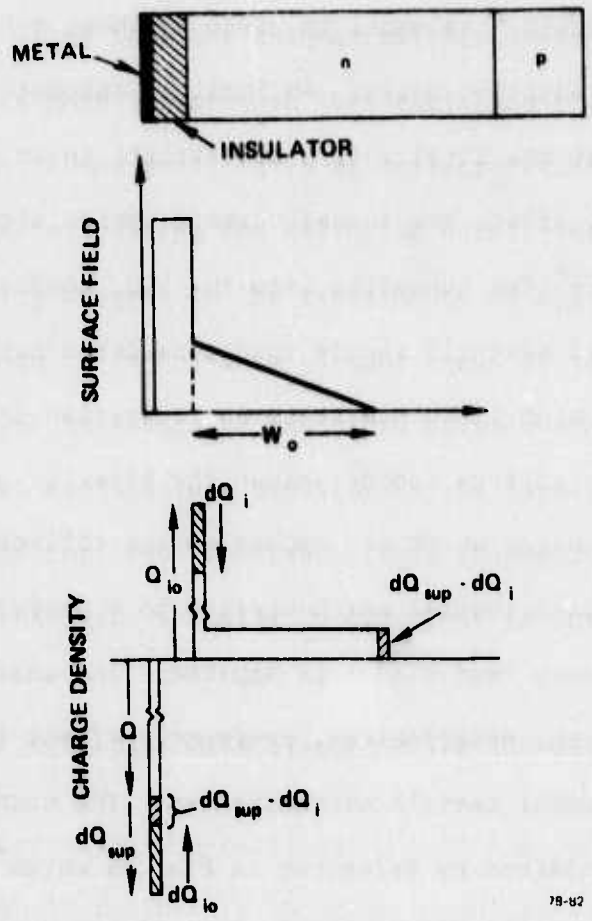

FIG. 33 Charge densities appearing on collector, inversion layer and edge of depletion layer in capacitance measurement.

ΔQ_m is annihilated by the increased hole conduction through the insulator, leaving a smaller net charge on the collector which must be balanced by an increase in depletion layer width.

Let E_s be the surface electric field in the semiconductor, ψ_s be the potential drop across the semiconductor surface, ϵ_s the dielectric constant of the semiconductor, Q_i be the charge density contained in the semiconductor inversion layer and p_s be volume density of ionized holes at the semiconductor surface. These quantities are related by the approximate relation

$$E_s^2 = \frac{2p_s kT}{\epsilon_s} + \frac{2qN_d}{\epsilon_s} |\psi_s| \qquad (2)$$

independently derived by Ong and Pierret[5] and by Green and Schewchun[2] in order to describe surface electric fields in nonthermal equilibrium depletion zones in MOS structures. E_s is also related to these quantities by Gauss' law

$$E_s = \frac{Q_i}{\epsilon_s} + \frac{qN_d}{\epsilon_s} W \quad . \qquad (3)$$

Neglecting the voltage drop across the inversion layer so that

$$|\psi_s| = \tfrac{1}{2} \frac{eN_d}{\epsilon_s} W^2 \quad , \qquad (4)$$

yields in combination with Eqs. (2) - (9)

$$p_s = \frac{1}{2kT}\frac{Q_1^2}{\epsilon_s} + \frac{e}{kT}\frac{Q_i N_d W}{\epsilon_s} \tag{5}$$

Equations (2) and (5) are derived implicitly from the assumption that the hole current density in the semiconductor is given by $J_p = - e\mu_p\, pD\varphi_p$, where μ_p is a (field-independent) mobility, p is the hole density and φ_p is the hole imref.

It is convenient to define

$$\left.\begin{aligned} p_s &= p_{so} + \tilde{p}_s\, e^{i\omega t} \\ Q_i &= Q_{io} + \tilde{q}_i\, e^{i\omega t} \\ W &= W_o + \tilde{W}\, e^{i\omega t} \\ \psi_s &= \psi_{so} + \tilde{\psi}_s\, e^{i\omega t} \\ J_{pt} &= J_{pto} + \tilde{j}_{pt}\, e^{i\omega t} \end{aligned}\right\} \tag{6}$$

where the symbols with a subscript zero are steady-state (dc) values of the variables and the symbols with a tilda are (small) ac magnitudes of the variables. From Eqs. (5) and (6) it follows that

$$p_{so} = \frac{1}{2kT}\frac{Q_{io}^2}{\epsilon_s} + \frac{gN_d}{kT\epsilon_s} Q_{io} W_o \tag{7}$$

and from Eqs. (4) and (6) that

$$|\psi_o| = 1/2\, \frac{eN_d}{\epsilon_s} W_o^2 \tag{8}$$

Neglecting terms which involve products of the ac quantities, Eq. (5) can be written

$$\tilde{p}_s = \frac{1}{kT\epsilon_s} Q_{io}\, \tilde{q}_i + \frac{eN_d}{kT\epsilon_s} (Q_{io}\, \tilde{W} + W_o\, \tilde{q}_i) \qquad (9)$$

We consider the situation in which a constant hole current density J_s is directed towards the semiconductor surface. Such a current can be supplied experimentally by biasing the emitter-base junction of the ICS with a constant current. Neglecting recombination of holes in the inversion layer with electrons which tunnel from the metal into the semiconductor, it follows from charge conservation that

$$\frac{dQ_i}{dt} = J_s - J_{pt} = J_o - \alpha p_s \qquad (10)$$

where we write J_{pt} as $J_{pt} = \alpha p_s$, where $\alpha = \dfrac{4\pi m_t\, e(kT)^2}{h^3\, N_v} \exp(-\eta)$ from

Eq. (1). Now $dQ_i/dt = i\omega\tilde{q}_i\, e^{i\omega t}$ and $\tilde{j}_{pt} = \alpha\tilde{p}_s$, so that

$$\tilde{p}_s = -\frac{i\omega}{\alpha}\tilde{q}_i$$

Substituting in Eq. (9) and using the fact that

$$\tilde{\psi} = \frac{eN_d}{\epsilon_s} W_o\, \tilde{W} \qquad (10)$$

we obtain

$$\left(Q_{io} + eN_d W_o - \frac{i\omega \epsilon_s kT}{\alpha}\right) \tilde{q} = - \frac{\epsilon_s Q_o}{W_o} \tilde{\psi} \qquad (11)$$

From Eq. (10) it follows that if we denote the incremental charge supplied to the collector by $\tilde{q}_{sup}$ then

$$\tilde{q}_{sup} = \tilde{q} + q N \tilde{\omega} = \tilde{q} + \frac{\epsilon_s}{\omega_o} \tilde{\psi} \quad . \qquad (12)$$

It is convenient to relate Eq. (11) to impedance formulas by using instead of $\tilde{q}$, current densities, and therefore

$$\tilde{j}_t = \frac{dq_{sup}}{dt} = i\omega \tilde{q}_{sup} \qquad (13)$$

where j_t represents the "total" current density (conduction and displacement current). From Eq. (11) - (13)

$$j_t = - i\omega \frac{\epsilon_s}{\omega_o} \left[1 + \frac{Q_o}{\left(Q_o + qN\omega_o - \frac{i\omega \epsilon_s kT}{\alpha}\right)}\right] \tilde{\psi} \quad . \qquad (14)$$

Equation (14) is in the form of $j = Y\psi$, where Y is an admittance so that $Y = - j\omega C + 1/R$. Equation (14) can be rewritten as

$$j_t = \frac{-i\omega\epsilon}{W_o}\left[1 + \frac{Q_o(Q_o + qN\nu_o)}{(Q_o + qNW_o)^2 + \frac{\omega^2\epsilon_s^2}{\alpha^2}k^2T^2}\right]$$

$$+ \frac{\omega\epsilon_s}{W_o}\left[\frac{Q_o\,\omega\,\epsilon_s/\alpha\;kT}{(Q_o + qN\nu_o)^2 + \frac{\omega^2\epsilon_s^2}{\alpha^2}\;k^2T^2}\right]$$

Therefore, we identify the shunt capacitance C_{11} and resistance R_{11} related to the admittance Y as

$$C_{11} = \frac{\epsilon_s}{W_o}\left[1 + \frac{Q_o(Q_o + qN\nu_o)}{(Q_o + qNW_o)^2 + \omega^2\epsilon_s^2/\alpha^2\;k^2T^2}\right] \tag{15}$$

$$R_{11} = \frac{\omega_o}{\epsilon_s}\;\frac{(Q_o + qN\nu_o)^2 + \omega^2\epsilon_s^2/\alpha^2\;k^2T^2}{Q_o\omega^2\,\epsilon_s/\alpha^2\;kT} \tag{16}$$

respectively.

If $\alpha \ll \frac{\omega\,\epsilon_s\;kT}{Q_o + qN\nu_o}$, then according to Eq. (15) $C_{11} = \frac{\epsilon_s}{\omega_o}$, the depletion layer capacitance and the inversion layer has no effect. It is reasonable that at a high enough frequency and small enough α no effect should be obtained because within a cycle of the applied frequency no significant charge can be transported across the insulator.

It is not immediately obvious that there should be some effect at 1 MHz. A significant effect on the capacitance will occur only if $\alpha \geq \omega \epsilon_s kT/qNW_o$. According to Eq. (1), $\alpha = 6.76 \times 10^{-13} e^{-\eta}$. Therefore, a change in capacitance can occur only if $e^{-\eta} = 4.64 \times 10^{-7}$ or $\eta = 14.6$ if $W_o = 1\ \mu m$ and the doping density is $5.3 \times 10^{15}\ cm^{-3}$. According to Habib and Simmons $\eta \approx 30$, so no change in capacitance should be observed with varying emitter current. Since significant changes are observed we must therefore prefer the smaller value of η. Such a small required value of η is not completely unexpected since, as pointed out by Card[1], the effective tunneling barrier height of the SiO_2 conduction band is a function of thickness for thermally grown oxides on silicon. Card plots η vs d for SiO_2 layers up to 23 Å. Extrapolating his experimental curve to high values of d, we expect that $\eta \approx 14.6$ at 25-27 Å. Our experimental value was 33 Å.

It is possible that the value of η in our experiments is lower than what would be expected because of perimeter currents which are larger because of the higher electric field which can lower the barrier height. Perimeter-dependent currents have sometimes been observed in these devices in their low impedance state as described in Appendix A. No direct proof of perimeter-dependent currents is available for the high impedance state.

C. CAPACITANCE OF ICS DEVICES IN LOW IMPEDANCE STATE

1. Method of Measurements

Capacitance data between 1-8 GHz were obtained on ICS devices using an HP network analyzer. The devices were mounted in varactor packages and two terminal capacitances measured (between the emitter and collector terminals). The method of separating the capacitance of the device from the parasitic mounting reactances was different from that previously used, however. Instead

of "disembedding" the diode from what, in detail, is a very complicated circuit requiring the accurate knowledge of from 3 to 12 components, a simpler approach was used. The impedance of the mounted diode was not compared to that of a standard short circuit, rather another identical varactor package was prepared which had the same number of leads as did the package containing the test device. The leads running from the lip of the package and bonded to the package base or device, were of the same length and relative position for both packages. Thus, this comparison mounting had the same circuits as the package containing the test diode except a short circuit was substituted for the device's intrinsic impedance. Assuming that the comparison "shorted package" is an ideal short circuit (and thereby treating the entire mounting circuit as an extra length of lossless transmission line) enables one to directly measure the impedance of the device without requiring specific accurate knowledge of what the mounting circuit is. This method cannot be used except at one frequency at a time since a new "short" reference must be obtained for each test frequency. However, since we are mainly interested in variations of device capacitance with applied bias, this is not a serious complication to the method.

A two-terminal capacitance was measured (the base terminal left open) in order not to complicate the disembedding procedure. The devices conveniently had an emitter area nine times their collector area. The emitter-base capacitance, as by direct measurement, was large compared to the emitter-collector capacitance if the devices were biased in their low impedance state. The resulting data are therefore reasonable respective to the collector portion of the device. (Collector-base capacitance was not measured since a low impedance state is not obtainable unless the emitter is supplied with current. The latter requirement would probably affect the accuracy of the data to a

greater extent than the assumption that the emitter-base capacitance can be compensated for in the measurement of emitter-collector capacitance.)

2. Measurements

The basic observations on device capacitance made in the low impedance state are summarized in Fig. 34, which also shows the measured capacitance of the device in its high impedance state. The collector-base voltage was determined by $V_{CB} = V_{CE} - V_{BE}$, where these voltages were measured as a function of current on the same three-terminal device used to measure the collector-emitter capacitance. The theoretical curves are calculated on the basis of standard MOS theory and represent the collector-base capacitance only. For thermal equilibrium, the capacitance per unit area is given if the semiconductor is given by

$$C_S = \frac{\partial Q_s}{\partial \psi_s} = \frac{\epsilon_s}{L_D} \frac{\left[1 - e^{-\beta\psi_s} + \frac{p_{no}}{n_{no}} \left(e^{\beta\psi_s} - 1\right)\right]}{F\left(\beta\psi_s, \frac{p_{no}}{n_{no}}\right)} \tag{17}$$

where Q_s is the charge per unit area delivered to the collector, ψ_s is the surface potential of the silicon, ϵ_s is the dielectric constant of silicon, L_D is the extrinsic Deybe length, $\beta = 1/kT$, where k is Boltzmann's constant and T is the absolute temperature and n_{no} and p_{no} are respectively the thermal equilibrium concentration of electrons and holes in the n layer of silicon adjacent to the insulator. Finally, $F(\beta\psi, p_{no}/n_{no})$ is defined by

$$F\left(\beta\psi, \frac{n_{po}}{p_{no}}\right) = \left[\left(e^{-\beta\psi} + \beta\psi - 1\right) + \frac{p_{no}}{n_{no}} \left(e^{\beta\psi} - \beta\psi - 1\right)\right]^{\frac{1}{2}} \tag{18}$$

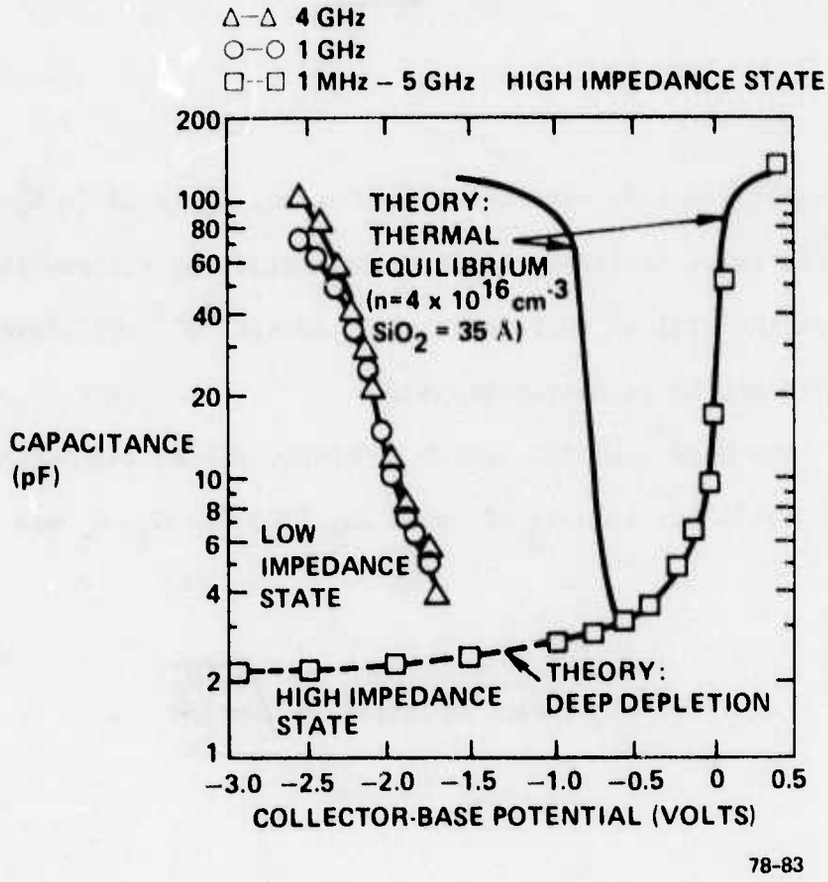

FIG. 34 C-V characteristics of Mo-SiO_2-n-p^+ device. Microwave frequency measurements made between emitter and collector and corrected by emitter junction capacitance and voltage drop.

The total capacitance C per unit area of the insulator layer C_i and silicon C_s is given by

$$C = \frac{C_i C_s}{C_i + C_s}$$

The theoretical curves were calculated on the basis of independent measurement of the oxide thickness of 35 Å (determined by ellipsometry) and a doping density in the silicon surface layer N_A of $4 \times 10^{15}/cm^3$ (determined by differential capacitance measurements).

The deep depletion (high impedance state) capacitance was calculated using Eq. (19), but instead of using Eq. (17) for C_s, C_s was taken as

$$C_s \text{ (deep depletion)} = \sqrt{\frac{q\epsilon_s N_A}{2\psi_s}} \quad .$$

Several observations are immediate:

(1) Deep depletion adequately describes the high impedance state (not a new result but already contained in our 1973 proposal). For biases above 0.5 V, the high impedance state departs radically from thermal equilibrium.

(2) The low impedance state is not at thermal equilibrium (hardly an earth-shaking result since current is being conducted through the device), but a simplistic interpretation would confirm that it represents a closer approximation to thermal equilibrium than does the high impedance state.

(3) The microwave capacitance in the low impedance state is not a rapidly varying function of microwave frequency. Data has been obtained

between 1 and 8 GHz but only two frequencies are shown for clarity. The largest differences in the data at different frequencies occur at high capacity and this likely represents experimental error more than a real physical effect. At $C \approx 100$ pF, the device looks so much like a short circuit that accurate impedance measurements are difficult. (An error of about 0.1 degree in phase of reflection could produce a change in capacitance of 20 pF at 4 GHz, for example, if $C > 100$ pF. The percentage error in measured C is much less for low values of C.)

There is a nontrivial nonlinear effect produced by microwave test frequency measurements, as described in the next section, and the complete description has not been completely unraveled at the higher microwave frequencies. This nonlinear effect produces a self-biasing (rectification-detection). It is felt that it has not contributed any significant uncertainty to the data of Fig. 34, however, for the following reasons:

(1) Data were obtained at the lowest microwave powers consistent with stable operation of the network analyzer.

(2) The nonlinear effect, as judged by changes produced in dc I-V characteristics, is much greater in the high impedance state.

(3) The nonlinear effect appears significantly smaller at higher microwave frequencies where study of the effect is more difficult.

SECTION 7

NONLINEAR EFFECTS OF MICROWAVE POWER ON ICS DEVICES

A. BACKGROUND

As mentioned previously in this report, care must be taken in the measurement of microwave impedances of ICS devices in that microwave power can affect the dc I-V characteristics of the devices. This section of the report describes these effects in detail and it is shown that microwave detection and threshold switch functions can be performed.

The data were all obtained from a standard device structure used for ICS, essentially the same as that diagrammed in Fig. 1. As a microwave detector this structure is not optimized. It had a large emitter area equal to 1.13×10^{-3} cm^2 and a collector area of 1.25×10^{-4} cm^2, both areas being large compared to standard microwave detector diodes. Construction of a more elegant microwave detector structure was not attempted as it was viewed as being too diversionary for our main goals. The purpose of this section is therefore threefold:

(1) To prescribe limits to the accuracy of microwave impedance measurements of these devices due to nonlinear effects.

(2) To report to whomever may be interested that a novel microwave detector and/or power threshold alarm exists and whose present performance may be no real indication of its potential sensitivity.

(3) To again provide reinforcement from a novel experimental arrangement for the basic model of inversion-controlled conduction as the mechanism responsible for ICS behavior.

B. THEORY

In the high impedance state, when a low bias is applied to an ICS diode, the emitter may have a higher differential resistance than the collector. Adding an ac signal to the dc bias can therefore result in a rectification; consequently, the increased injection of minority carriers into the base can lower threshold voltages and change high impedance state C-V characteristics. These changes are observed to depend upon the rf power used to perform the measurements.

In this respect, the effect of microwave power is quite similar to optical excitation on the device. Both optical excitation and microwave excitation face an increased bias on the emitter-base junction. This results in: (1) a shift of the low-voltage C-V characteristics by 0 - 0.4 V (depending upon the intensity of light or the microwave power used); (2) a change in I-V characteristics which is manifest at low voltages by increased conduction through the device which would normally appear at a voltage 0 - 0.4 V bias in the opposite direction (the extent of shift depends again on the optical intensity or microwave power used; and (3) a lowering of the device threshold voltage. The effect of microwave power on the device is therefore a further confirmation of the inversion-controlled conduction model which predicts a lowered threshold voltage if an increased supply of minority carriers is available to be supplied to incipient inversion layers at the insulator-semiconductor interface.

C. MEASUREMENTS

The data of Fig. 35 show the variation of device threshold voltage with applied microwave power. These measurements were made with a test signal whose frequency was 2.0 GHz using the apparatus diagrammed in Fig. 36.

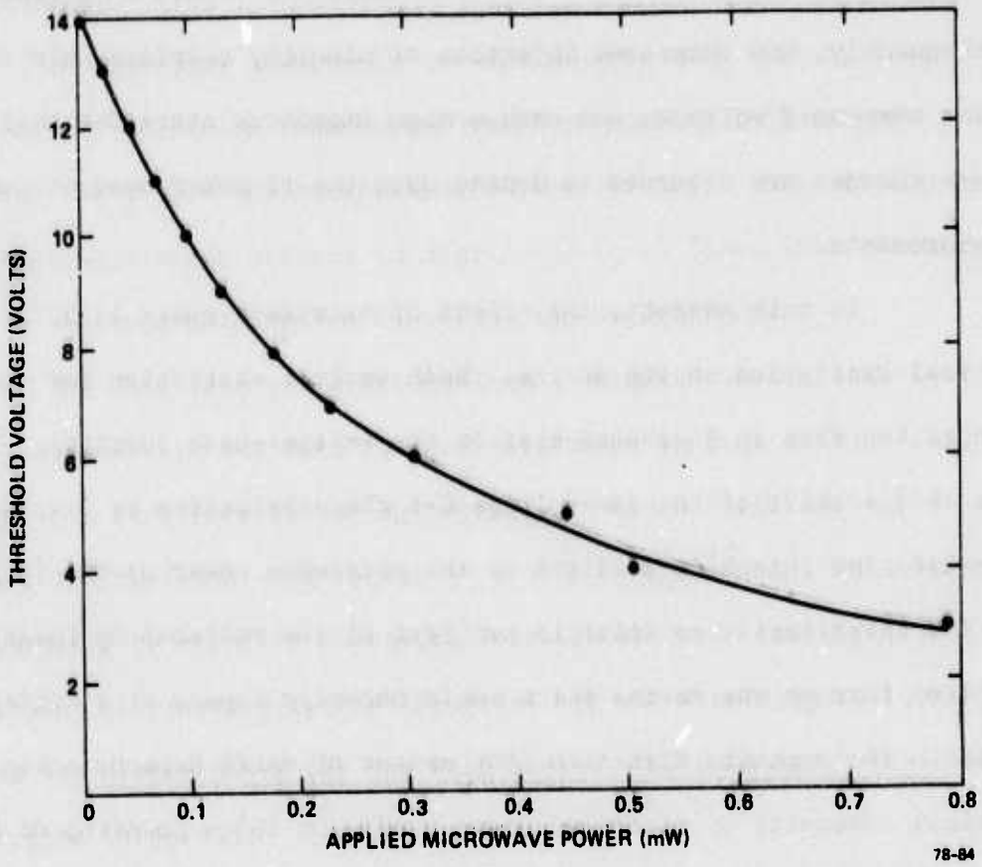

FIG. 35 Variation of Mo-SiO_2-n-p^+ device's threshold voltage as a function of microwave power supplied at 2.0 GHz.

The double stub tuner was used to match the device to source. The device was a Mo-SiO_2-n-p^+ structure with an emitter area of 1.13×10^{-3} cm^2 and collector area of 1.25×10^{-4} cm^2. The given amount of microwave power shown as the abscissa was sufficient to cause a transition to the low impedance state if the ordinate voltage was supplied to the device. Thus, a latching transition occurred. (The device remained in the low impedance state after the microwave power was turned down.) Similar, optically induced transitions have been observed. The relationship between the change in threshold voltage ΔV_{TH} and the microwave P appears to have roughly the form

$$\Delta V_{TH} = a\ P + b\ P^n$$

where a and b are constants and n is a number approximately equal to 2. Further work would be necessary to more precisely define n.

The experimental situation for which these data were obtained represents the operation of a microwave threshold alarm. A transition to the low impedance state will occur following the attainment of a certain level of received microwave power.

The device can also function as a more conventional detector without a latching transition. A simple way to prohibit a latching transition is by increasing the load resistance of Fig. 36 device sufficiently that no transition to the low impedance state can take place. A sufficiently high value of R_L is assured if

$$R_L > \frac{V}{I_s}$$

where V is the supply voltage and I_s is the low impedance state sustaining current. An alternate method of preventing a transition to the low impedance state is to bias the device with a current source whose output current is less than I_s.

The change in voltage across the device which occurs when a given amount microwave power is applied will clearly depend upon the method of biasing the device (if a transition to the low impedance state is avoided). In order to present data which will enable the calculation of how much voltage swing would occur for any method of biasing the data of Fig. 37 are presented. These show the I-V characteristics of a device in its high impedance state for various amounts of applied microwave power. A greater microwave power causes a larger current at the small applied voltage. One would not expect that these characteristics are essentially different from what might be obtained from a conventional bipolar transistor with connections made only to its emitter and collector terminals (base left floating).

The data of Fig. 37 were obtained at a 1 GHz test frequency from a Mo-SiO_2-p-n^+ device of the same area as the Mo-SiO_2-n-p^+ device whose behavior as a threshold switch was described in Fig. 14. The p-type base layer of the p-n^+ devices was significantly thicker ($\approx$ 7-8 μm) than the n-type base layer of the n-p^+ device ($\approx$ 2 μm).

The curves of Fig. 37 show that if, say, a 20 μA current bias is used, the voltage on the device would change from 8 V to 3 V, if a 7 mW of 1 GHz power were applied to the device. Removing the microwave power would cause the voltage to swing back to 8 V.

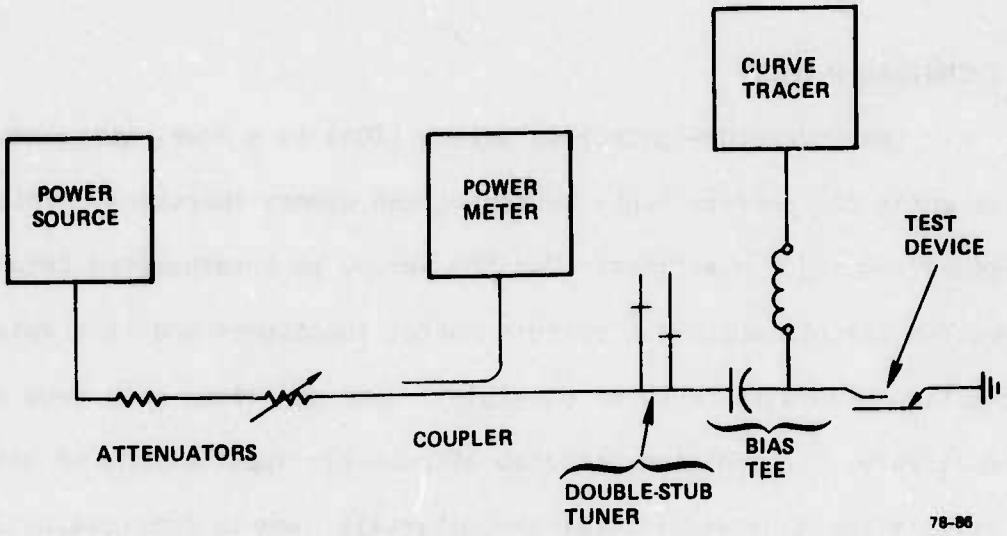

FIG. 36 Diagram of apparatus used to obtain data of Fig. 35.

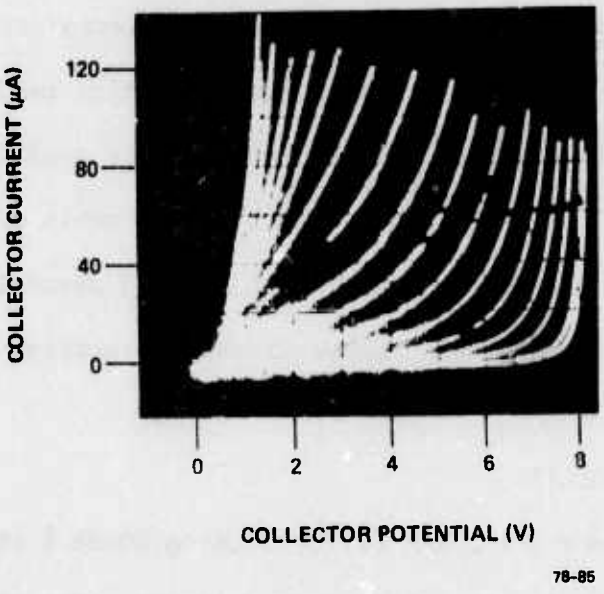

FIG. 37 I-V characteristics of a Mo-SiO_2-n-p^+ device in high impedance state with various amounts of 1 GHz microwave power applied.

SECTION 8

SUMMARY OF REPORT

A. TECHNICAL PROBLEM

The inversion-controlled switch (ICS) is a novel semiconductor device which can perform rapid switching and memory functions. This program addressed two major questions: Can the device be incorporated into an integrated circuit which can perform useful functions; and is a detailed explanation of device behavior possible? Both questions have been answered affirmatively. In addition, studies of possible applications of discrete ICS devices and studies of insulator materials used in fabricating ICS were conducted.

B. GENERAL METHODOLOGY

Devices were fabricated and tested with wide structural variations and their performance compared with theory. Memory arrays suitable as static random-access memories (RAM's) with nondestructive readout and which have only a single active device per memory site were constructed using discrete devices in order to demonstrate a functional circuit design. The circuit which showed the most ideal behavior in a 3 x 3 discrete array was translated to an integrated format using conventional integration techniques.

C. TECHNICAL RESULTS

Undecoded 2 x 2 RAM circuits using 30-35 Å SiO_2 conducting insulator layers were fabricated in an integrated format. The basic fabrication process is compatible with simple bipolar techniques and probably superior performance (in terms of area density and power consumption) could be achieved

using the more advanced dielectric isolation technique used in modern bipolar circuit designs. Holding powers less than 2 μW per bit are projected to be obtainable with small area device designs and total power consumption for an ICS RAM should be less than for an MOS memory of comparable number of bits. Read access time of the ICS should be much less than MOS memories, however.

Current-voltage and capacitance-voltage characteristics of devices can be explained by detailed application of the simple device model developed under earlier contractual support.

Several types of ICS devices were subjected to transient radiation at RADC, Solid State Science Division, Hanscom Field using a 10 MeV electron beam. Most devices would lose information in a RAM-type circuit at radiation dose rates between 10^8 and 10^9 rads (Si)/s. However, one structure, a Mo-SiO_xN_y-p-n^+ device, was found to hold information at radiation dose rates of the order of 10^{10} rads (Si)/s.

D. DOD IMPLICATIONS

The demonstration of an integrated ICS RAM, even on the small scale attempted, shows that the ICS is, in principle, integratable. The high speed and small power consumption of the ICS may make a full-scale memory circuit development profitable for special applications.

The radiation hardness of the SiO_xN_y insulator device may permit the development of a new class of radiation-hard semiconductor memories.

E. IMPLICATION OF FURTHER RESEARCH

The experiments on radiation hardness were undertaken as an aside to further establish and test theories of device operation. The radiation hardness of devices employing silicon oxynitride insulator layers was not

completely expected and is only partially explained at present. Further research may be warranted on this aspect of ICS behavior to help determine if an ICS radiation-hard memory is worth developing. A primary problem such research should address is the power consumption requirements for a radiation-hard memory which probably will be greater than that for alternative radiation-sensitive ICS memory arrays.

APPENDIX A

Steady-State Characteristics of Two Terminal Inversion-Controlled Switches*

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* Supported in part by the Defense Advanced Research Projects Agency and monitored by Rome Air Development Center, Deputy for Electronics Technology, under Contract No. F19628-76-C-0105.

Steady-State Characteristics of Two Terminal Inversion-Controlled Switches*

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A B S T R A C T

The important fabrication procedures and the direct current-voltage characteristics of metal/conducting "insulator"/semiconductor junction diodes are described. These devices generally have two impedance states. The high impedance state is associated with a steady-state deep depletion of the semiconductor surface which permits the device to absorb a high voltage. The low-impedance state is associated with a partial inversion of the semiconductor surface which greatly increases the electric field across the insulator, even though only a low voltage exists across the device. The generality of this phenomenon is emphasized by citing results from a wide variety of combinations of insulator materials and semiconductor structures. Uniformity of conduction through the insulator and ruggedness of the device are discussed in detail. The device's I-V characteristics can either be independent or quite sensitive to ambient temperature. The temperature sensitivity is explained by the effects of temperature on those mechanisms which control the formation of inversion layers.

* Supported in part by the Defense Advanced Research Projects Agency and monitored by Rome Air Development Center, Deputy for Electronics Technology, under contract No. F19628-76-C-0105.

LIST OF SYMBOLS

A^* - Effective Richardson constant

C - Capacitance

D - Diffusion constant (cm^2/sec)

I - Current (A)

I_C - Collector current

I_{min} - Minimum current in intermediate impedance state

I_{max} - Maximum current in intermediate impedance state

I_S - Sustaining current in low impedance state

I_{TH} - Maximum current in high impedance state

J - Current density (A/cm^2)

k - Boltzmann's constant

N - Ionized donor (or acceptor) density

q - Electronic charge

R - Resistance (ohms)

R_L - Collector load resistance

T - Temperature (^oK)

V - Potential (volts)

V_A - Avalanche breakdown voltage

V_B - Barrier voltage

V_d - Voltage across depletion layer

V_g - Silicon bandgap voltage

V_{EB} - Emitter-base voltage

V_{EC} - Emitter-collector voltage

V_i - Voltage across insulator

V_{in} - V_{EC} for intermediate state

V_S - Sustaining voltage (minimum V_{EC} in low impedance state)

V_{TH} - Threshold voltage

W_B - Base width (cm)

W_d - Depletion layer width (cm)

α - Constant in Frankel-Poole law ($(eV)^2/V$)

ϵ_S - Dielectric constant of silicon (F/cm)

φ_p - Hole barrier height (V)

γ_t - Trap depth (V)

I. INTRODUCTION

The existence of bistable impedance states has previously been reported in metal/conducting-"insulator"/n/p^+-silicon diodes [1], [2] and in metal/conducting-"insulator/p/n^+-silicon diodes [3], when voltage is applied in the sense which forward biases the p-n junction and depletes the semiconductor surface, as shown in Fig. 1. Three-terminal versions of these structures in which electrical contact is made to the metal and both sides of the junction have shown dc current-voltage (I-V) characteristics similar to those of a silicon-controlled rectifier [3]-[5]. The third intermediate terminal is shown as a dashed line connection to the devices of Fig. 1. This paper will more completely describe the dc behavior of two-terminal devices, and indicate the generality of this phenomenon as it has been observed in a wide range of structural variations. (The following paper [6], hereafter referred to as "II," will cover the behavior of the three-terminal devices.) In addition, further experimental evidence will be offered which supports the proposed explanation of this phenomenon as inversion-controlled conduction across the insulator [2]. The emphasis of this paper is descriptive; a quantitative analysis of device behavior will be published elsewhere.

The inversion-controlled conduction model of device behavior associates the presence or absence of a low-impedance state with the presence or absence of an inversion layer at the semiconductor surface. A high impedance state can exist for these devices because of the finite conductivity of the insulator which prevents the build-up of an inversion layer. A high voltage can therefore be applied to the device because the surface depletion layer can have a steady-state equilibrium width which is much greater than that obtained in thermal equilibrium. The energy band structure and relative widths of the surface's and junction's depletion zones for a M/I/p/n device in its high

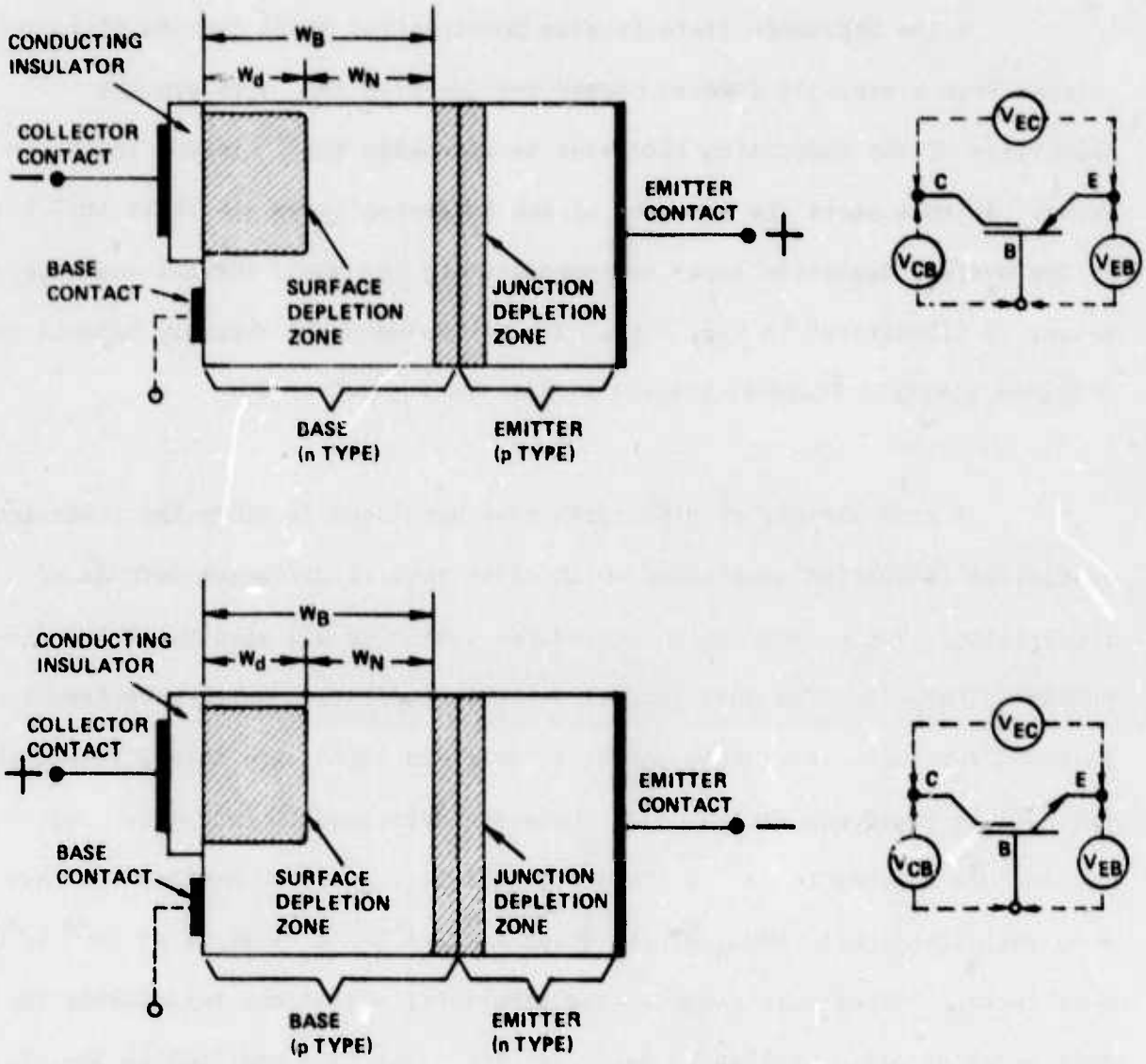


FIG. 1 Structure of inversion-controlled switches and proposed circuit symbols. Diagrams also illustrate definitions of base width W_B, surface depletion layer width W_d and neutral layer width W_N. Top: M-I-n-p device and symbol with definition of terminal potential differences. Bottom: M-I-p-n device and symbol.

impedance state are diagrammed in Fig. 2(a). The existence of steady-state deep depletion in MIS structures, which have conducting insulator layers but no p-n junction, has been studied previously; thin SiO_2 layers on Si have been investigated by Kar and Dahlke [7] and by Dubey et al. [8], for example.

A low impedance state is also possible for these devices since the current from a strongly forward biased p-n junction can overwhelm the capability of the conducting insulator to discharge the incipient inversion layer. In this state the presence of the inversion layer can limit the width of the surface depletion layer to approximately its small thermal equilibrium value, as illustrated in Fig. 2(b). The device conducts strongly because now a higher electric field is present within the insulator [2].

A wide variety of structures have been used to study the inversion-controlled conduction phenomenon which often require different methods of fabrication. Those fabrication procedures common to all structures are discussed in Sec. II. The most general I-V characteristics which have been observed for these inversion-controlled switches (ICS) show three, rather than two, stable impedance states [3]. These are described in Sec. III. The temperature dependence of the threshold voltage V_{TH} of ICS devices can have wide variations, with $|dV_{TH}/dT|$ as great as 1 V/°C and as small as 10^{-2} V/°C over certain temperature ranges. The structural variations responsible for this behavior are described in Sec. IV. The paper is summarized in Sec. V.

II. BASIC STRUCTURES AND FABRICATION

The properties of the two basic inversion-controlled switch (ICS) structures shown in Fig. 1 are qualitatively similar. Although use of a particular insulator material may make either the n-p or p-n structure easier to fabricate, no basic asymmetry has been observed in the I-V characteristics

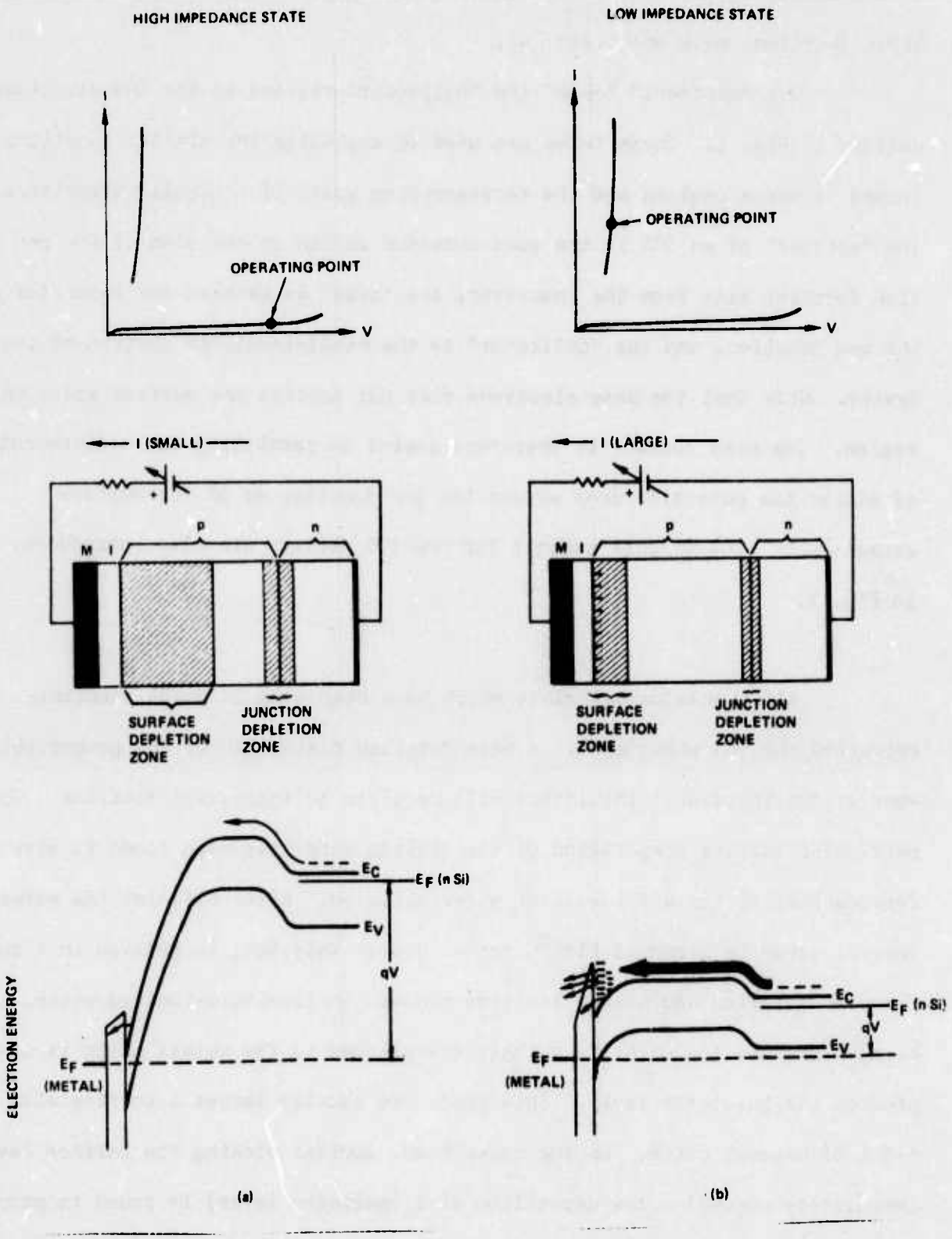


FIG 2 Bistable current-voltage characteristics, relative widths of surface and junction depletion zones and energy band diagram of M-I-p-n device. E_F, E_C and E_V denote Fermi level, conduction band edge and valance band edge, respectively.
(a) High impedance state.
(b) Low impedance state.

of the complementary semiconductor structures [3]. Both diffused and epitaxially grown junctions have been used [4].

The "emitter," "base" and "collector" regions of the ICS structure are defined in Fig. 1. These terms are used to emphasize the similar functions performed by these regions and the corresponding parts of a bipolar transistor [3]. The "emitter" of an ICS is the semiconductor region on the side of the p-n junction furthest away from the insulator; the "base" is between the insulator and the p-n junction, and the "collector" is the metal-insulator portion of the device. Note that the base electrode does not contact the surface space charge region. The base contact is therefore useful in permitting the measurement of either the potential drop across the p-n junction or of the surface capacitance. The circuit symbols for the ICS devices are also introduced in Fig. 1.

All insulator materials which have been used in these structures have evidenced the ICS phenomenon. A more detailed discussion of the properties of some of the individual insulators will be given in subsequent sections. One particular surface preparation of the silicon wafer has been found to give good reproducibility for all insulator materials used. After cleaning the wafer, a thermal oxide is grown at 1150°C for an hour. This SiO_2 is removed in a buffered HF solution and washed for five minutes in flowing deionized water. After being blown dry the wafer is quickly transferred to the vessel which is used to produce the insulator layer. This procedure usually leaves a surface with only 6-8 Å of nascent oxide. On the other hand, sputter etching the surface (even immediately preceding the deposition of a sputtered layer) is found to produce an exceptionally poor surface for all insulator materials used.

It is important that the insulator layer should present neither too high nor too low an impedance to current flow. The resistance of the insulator

must not be so great that an inversion layer can form in a conventional metal-insulator-semiconductor (MIS) structure, fabricated from the same insulator, but with no junction present in the semiconductor. Thus, for example, if SiO_2 is used as the insulator material, a 20-60 Å thickness is useful for the fabrication of ICS devices, whereas 100 Å of thermally grown SiO_2 would produce too perfect an insulator to permit significant conduction. Similarly, the insulator must not be too conductive. For example, a 20 Å thick layer of high conductivity silicon-rich, silicon nitride would not be able to support an inversion layer at the "insulator"-semiconductor surface, even under the influence of an adjacent forward-biased junction. However, thicker silicon-rich, silicon-nitride layers (from 60 Å to 400 Å thick) are quite useful as ICS "insulators."

Table 1 lists the properties of some of the insulator materials which have been extensively used to fabricate ICS's. The comments include the important fabrication procedures and performance properties of devices made with the particular insulators. (The symbols "I_S" and "V_S" are defined in Sec. III B and Fig. 4.)

Satisfactory collector metallizations have been achieved with a variety of metals including chromium, aluminum and molybdenum. These metals are not useful for all insulator layers, however, with the exception of molybdenum. Electron-beam evaporated or rf-sputtered (using less than 2 W/cm^2 power density) layers of molybdenum have produced excellent devices in all structural variations. For many insulator materials it is desirable to apply the collector metallization immediately after the insulator layer has been formed.

III. I-V CHARACTERISTICS

A. Two and Three Stable Impedance States

The I-V characteristics which are observed when electrical connections are made to the emitter and collector terminals (the base contact is left open)

Table 1. Properties of Insulator Materials Used in ICS Devices

		Deposition or Growth		
Insulator	Thickness Range (Å)	Method	Substrate Temperature (° C)	Comments
SiO_2	20–70	Thermal oxidation in dry O_2	550–700	M/SiO_2/n/p structures yield slightly lower I_s than do M/SiO_2/p/n devices.
SiO_2	30–45	Thermal oxidation in steam	550	Devices less reproducible than dry O_2 growth.
SiO_2	30–45	Sputtered	≈ 20–80	Pinhole density limits utility.
SiO_xN_y (index of refraction at 5460 Å = 1.65)	15–60	CVD	700	Highest observed yields in simple structures. Lower V_s observed in M/I/p/n devices than in M/I/n/p.
SiO_xN_y (index of refraction at 5460 Å = 1.8)	70–400	CVD	700–750	Intermediate impedance state common.
Si (amorphous)	200–2000	Sputtered	≈ 30–100	Devices extremely sensitive to surface preparation and sputtering conditions.
Si (undoped polycrystalline layer)	10^3–10^4	CVD	700–750	Excellent reproducibility; intermediate impedance state not observed.
Ge (amorphous)	40–400	Evaporation from Mo boat	≈ 30–70	Lowest I_s observed; devices extremely sensitive to surface preparation; better devices observed using Mo rather than W evaporation boat.

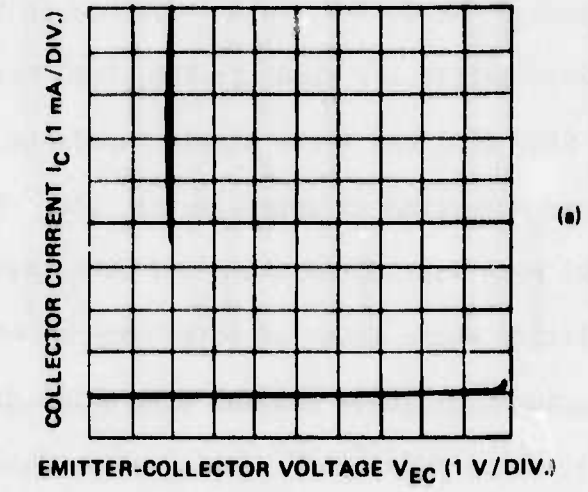
reveal important properties of ICS devices. At least two and at most three stable impedance states are observed [3]. The detailed description of I-V characteristics showing three stable impedances has not been previously reported.

Figure 3 presents the dc I-V characteristics of two different ICS's. The device whose characteristics are shown in Fig. 3(a) has only two impedance states; the device of Fig. 3(b) has three stable impedance states with the third intermediate state occurring at approximately 11V. Both the devices of Fig. 3(a) and Fig. 3(b) were fabricated using the same insulator material (30 Å of silicon oxynitride whose index of refraction at 5640 Å is 1.7 [2]). The semiconductor structures of these devices were quite different, however. The device of Fig. 3(a) was a $M/I/p^+/n/n^+$ device whose junction was formed by the diffusion of boron into an n-type epitaxial layer grown on an n^+ substrate. The device of Fig. 3(b) was a $M/I/p/n^+$ structure whose junction was formed by epitaxial growth of a 10 ohm-cm p-type epitaxial layer on an n^+ substrate.

The term "stable impedance state" as used here comprises three conditions: (1) A region of positive differential resistance exists on a I-V plot; (2) This region of positive differential resistance must be observable with direct current; and (3) The I-V characteristics must be recyclable.

No universal rule has been discovered which allows the prediction of whether or not the intermediate impedance state will be present for all variations of device parameters. However, several rules which have limited validity for certain semiconductor structures or particular insulators have been inferred from extensive experimentation with the fabrication of many ICS structural variations. These include the absence of the intermediate impedance state in all devices which either have polycrystalline silicon as the insulator or in most devices which have either diffused bases or low threshold voltages.

The origin of the intermediate level impedance state is not clear. Careful study of the C-V characteristics of devices in their high impedance



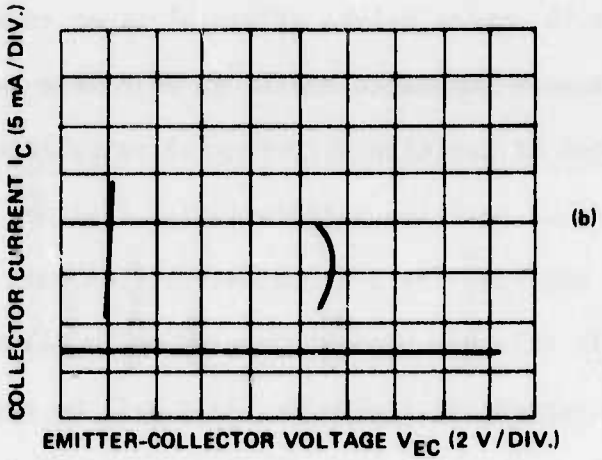


FIG. 3 I-V characteristics of ICS diodes.
(a) Two stable impedance states of a metal-silicon oxynitride-p^+-n-n^+ device.
(b) Three stable impedance states of a metal-silicon oxynitride-p-n^+ device.

state has shown that there is no anomaly near the voltage at which the intermediate impedance state appears. Thus, it is not possible to associate the intermediate impedance state with some intrinsic property of the insulator to partially invert at some particular applied voltage when the surface is in a "deep" (nonthermal equilibrium) depletion [8].

B. Critical Currents and Voltages

1. Threshold voltage and current. The maximum voltage which can be applied to the collector when the device is in its highest impedance state is called the threshold voltage V_{TH}. Threshold voltages as low as 1.5 V and as high as 70 V have been observed in different device structures. The most important factors which determine V_{TH} are the doping level and thickness of the base [2], and the conduction properties of the insulator layers.

Figure 4 displays I-V characteristics of an ICS diode. This diagram provides a graphical definition of V_{TH} as well as the maximum current I_{TH} which the device can carry in its high impedance state, which occurs at V_{TH}. The total voltage V_{EC} applied across the device may be divided up into the potential differences across the insulator V_i, across the surface depletion zone V_d, and across the junction V_{EB}:

$$V_{EC} = V_i + V_d + V_{EB} \quad ,$$

where the voltage drop across any inversion layer which might be present is neglected. For a uniformly doped base-region

$$V_d = 1/2 \frac{qN}{\epsilon_S} W_d^2 \quad ,$$

where N is the assumed uniform ionized donor (or acceptor) density of the base, q is the electronic charge, ϵ_S is the dielectric constant of silicon and W_d is

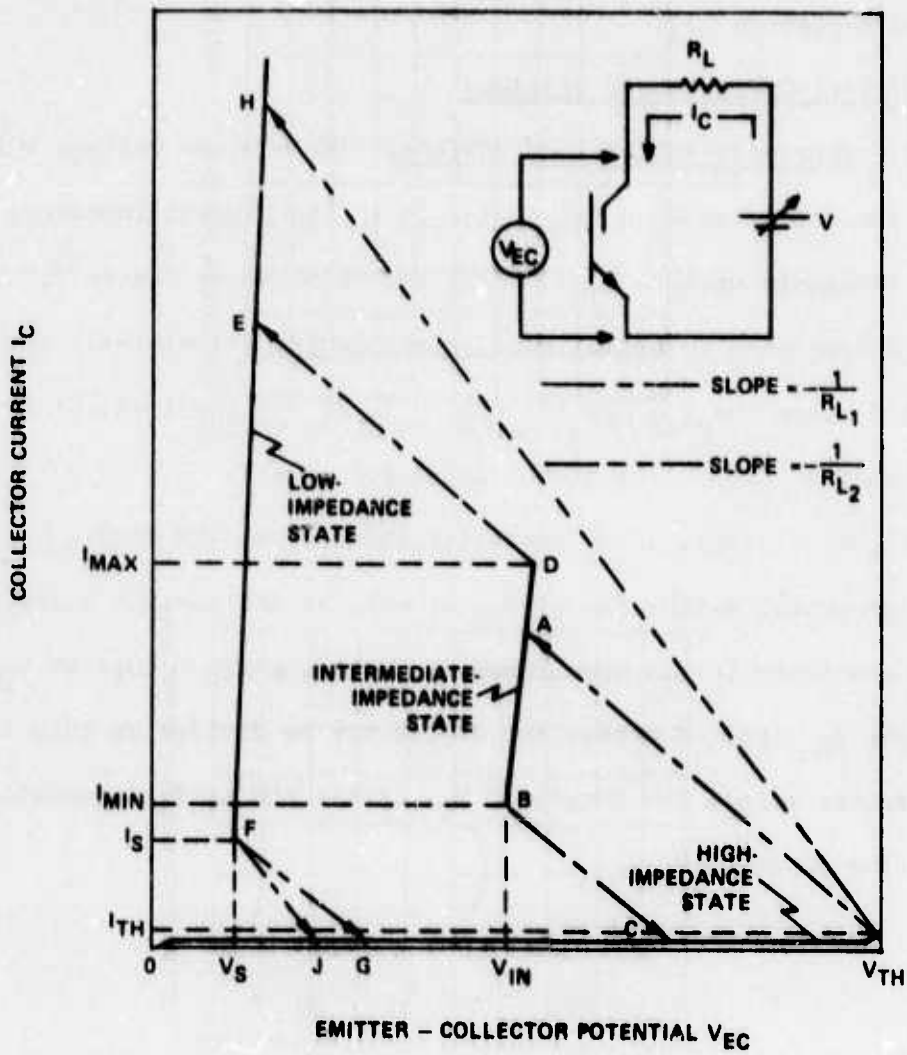


FIG. 4 Definition of critical currents and voltages of ICS diode having three stable impedance states. Load lines show possible transitions between states for unilluminated diode. Note that with a low value of collector load resistance, the intermediate state may not be accessible.

the width of the depletion zone, as shown in Fig. 1. The voltage drop across the semiconductor depletion zone, when the surface depletion zone "punches through" to the emitter junction depletion zone, is given by

$$V_p = 1/2 \frac{qN}{\epsilon_S} W_B^2 \quad ,$$

where W_B is the width of the base region measured from the semiconductor surface to the edge of the emitter junction depletion layer, as shown in Fig. 1. Punch through is possible only for base regions sufficiently thin and/or lightly doped that avalanche breakdown of the semiconductor does not occur at a lower voltage than V_p.

Clearly, if V_d is equal to V_p, strong injection of minority carriers from the emitter will occur. Thus, an upper limit of V_{TH} exists for lightly doped and thin base regions and is given by

$$V_{TH} \leq V_i + V_p + V_{EB} \tag{1}$$

since such a bias would ensure development of an inversion layer for all insulators used in ICS devices. For all devices studied it was found that at room temperature V_{TH} is below the limit of Eq. (1) and is observed to be

$$V_{TH} < V_p, \tag{2}$$

and for most insulators it is often observed that $V_{TH} < \frac{1}{2} V_p$. (V_p may be determined by measuring the collector-base capacitance as a function of applied collector-base voltage if the emitter terminal is left open. As will be discussed in II, inversion does not occur with such a bias arrangement with insulator layers conductive enough to be used in ICS devices.)

For more heavily doped base regions, the upper limit of V_{TH} will be given by

$$V_{TH} < V_i + V_A + V_{EB} \quad ,$$

where V_A is the avalanche breakdown voltage of the surface depletion layer. Devices whose $V_A < V_p$ have a markedly smaller dependence of V_{TH} upon ambient temperature and this will be discussed in Sec. IIC.

The inequality of Eq. (2) is readily understood. With terminal connections to only the emitter and collector the base will acquire a potential intermediate between that of the emitter and collector, thus slightly forward biasing the emitter. It is observed that V_{EB} is a monotonically increasing function of V_{EC}. Neglecting recombination in the neutral region of the base, the current density of minority carriers J_p injected into the base will vary approximately as

$$J_p = \frac{qD}{W_B - \left(\frac{2V_D\epsilon_S}{Nq}\right)^{\frac{1}{2}}} p_o \exp\left\{\frac{qV_{EB}}{kT}\right\} \quad , \tag{3}$$

where D is the diffusion coefficient of minority carriers in the base, p_o is their thermal equilibrium concentration at the edge of the emitter junction depletion zone, k is Boltzmann's constant, and T is the absolute temperature. The quantity

$$\left\{W_B - \left(\frac{2V_D\epsilon_S}{Nq}\right)^{\frac{1}{2}}\right\} = (W_B - W_d) = W_N \quad ,$$

which appears in the denominator of Eq. (3), is the width of the neutral

region between the surface's and the emitter junction's depletion zones as defined in Fig. 1. Because raising V_{EC} will result in an increase in both V_d and V_{EB}, it is clear that J_p will increase with V_{EC}. The threshold voltage is attained when J_p increases to the point where the rate of arrival of minority carriers at the surface exceeds the capability of the surface to remove them by either direct transport across the insulator or by recombination. This can occur at applied voltages well below V_p [2].

The increased injection caused by a wider surface depletion zone is similar to an Early conductance in conventional bipolar transistors [9]. Equation (3) also serves to explain why devices fabricated with thinner epitaxial layers (smaller W_B) and lighter doping of their base regions (smaller N) will have a reduced V_{TH} even though punch through is never actually achieved [2].

Several runs of devices including $M/SiO_2/n/p^+$ and M/a - Si/p/n^+ structures have been fabricated for which V_{TH} is nearly equal to V_p. Some of these devices were distinguished by their insulator layers' extremely low conductivity. Compared to devices with higher conductivity insulator layers, the floating base potential therefore tends to remain much closer to the emitter potential as V_{EC} is increased. Thus, the injection of minority carriers is greatly limited until punch through is nearly obtained. An exact prediction on the effect of varying insulator layer composition and thickness upon V_{TH} is difficult to make because little is known regarding the ratio of electron-to-hole conduction currents across most insulators, especially under conditions of depletion of the semiconductor surface.

V_{TH} is also affected by surface state density, trapped charge near the semiconductor-insulator interface, and changing the collector metallization. These factors appear to influence V_{TH} by as much as 20% when room temperature measurements are made.

2. Virgin state. When switched for the first time many devices show a threshold voltage higher than that observed on all subsequent switching events. Devices which evidence this virgin state nevertheless have well defined V_{TH}, with all devices on a wafer having their V_{TH} within a 10% range, both before and after the first switching event. No further change in V_{TH} is usually observed after the first switching event, which typically reduces V_{TH} by about 20%.

Certain device structures do not have a virgin state. Among these are devices fabricated using polysilicon as the insulator layer and most devices fabricated by a procedure in which a phosphorus glass is formed on the thin insulator side of the wafer as the last high temperature (> 1000°C) step, before formation of the conducting insulator. Using such procedures the virgin state was not observed with either thermally grown SiO_2 or CVD silicon oxynitride devices, although companion structures, fabricated identically except for the phosphorus glass anneal, evidenced the virgin state, thus suggesting that the phosphorus glass acted as a getter for active impurities.

The erasure of the virgin state is believed to be caused by a permanent filling of deep traps within the insulator or at the semiconductor surface. Similar initial cycle events have been observed previously: for example, in capacitance measurements of silicon nitride memory devices [10] and in conductivity studies of silicon nitrides used in MNOS transistors [11]. The original virgin state threshold voltage has not been observed to be restored by temperature-bias stressing for most structures, thus these devices do not appear useful as nonvolatile memory devices.

Evidence for charge storage as the mechanism of erasure of the virgin state for at least some ICS structures can be obtained from a comparison of the C-V characteristics of devices in their virgin and nonvirgin states. The run of devices which showed the largest change in their C-V characteristics after the initial switching event were $M/SiO_2/n/p^+$ structures and their collector-base C-V

characteristics are shown in Fig. 5. The thickness of the thermal SiO_2 layer was determined to be 30 Å by ellipsometric measurements, and the calculated oxide capacitance for these devices, which had an area of 1.27×10^{-4} cm^3, was 125 pF. The voltage offset of approximately 0.3 V represents an increase in stored positive charge in the insulator. Storage of positive charge near the Si-SiO_2 interface has also been observed in conducting SiO_2 films by Weinberg [12] using metal/SiO_2/silicon devices which have no junction.

3. Lower impedance states. Figure 4 also illustrates the definition of the sustaining current I_S, which is the minimum dc current which can exist in the device's lowest impedance state. The sustaining voltage V_S is the voltage drop across the device in its lowest impedance state when $I = I_S$. Current densities corresponding to I_S of 1.6 A/cm^2 have previously been reported for ICS devices with polysilicon insulators [3]. The lowest value of current density of I_S observed was 0.4 A/cm^2 for a M/amorphous germanium/p/n^+ structure. Typical values of V_S are between 1.2 and 3 V. Diffused base devices with silicon oxynitride and amorphous germanium insulators have been observed with V_S = 1.1 V; epitaxially grown junction structures with polysilicon insulators have been observed to have V_S = 1.2 V [3].

The lowest impedance state has no upper limit of current which may be passed through the device other than that which may damage the device. Typical devices can pass in excess of 10^3 A/cm^2 without damage; one run of devices fabricated using silicon-rich, silicon nitride passed direct currents for several hours without damage with current densities in excess of 8.3×10^3 A/cm^2 when the 50 μm thick chips were soldered to copper heat sinks which were kept at 25°C ambient temperature.

In the intermediate impedance level state, however, there is both an upper and a lower limit to the current which is possible. Attempts to increase

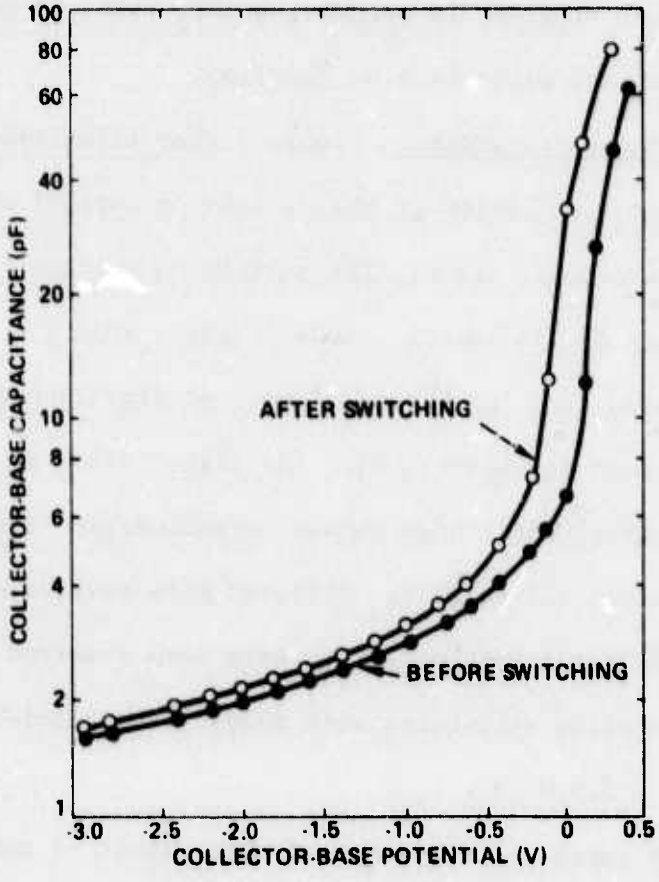


FIG. 5 Collector-base capacitance of a metal-SiO_2-n-p^+ device as a function of applied potential.

the current density above the upper limit (above about 12 mA for the device of Fig. 3(b)) result in a transition to the lowest impedance state. The upper limit of current density for the intermediate impedance state has been observed to be as low as 5 A/cm^2 and as large as 50 A/cm^2 for devices studied to date. This maximum current which can exist in the intermediate state is called I_{max}; the minimum current is called I_{min}. I_{min} is usually found to be less than I_S for the same device. The approximate voltage at which the intermediate impedance level occurs will be denoted by V_{in}. Typical devices in which an intermediate level impedance state is observable have $6\ V < V_{in} < 12\ V$.

C. Load Line Effects and Optically Triggered Switching

The switching of an ICS diode from one impedance state to another is partially determined by the load resistance R_L which is placed in series with the device and a voltage source. Consider a specific value of $R_L = R_{L1}$, where

$$R_{L1} \gtrsim \frac{V_{TH} - V_{in}}{I_{max}} \quad . \tag{4}$$

If the source voltage V shown in the insert to Fig. 4 is increased from zero, the device will remain in the high impedance state until the collector voltage V_{EC} reaches V_{TH}. Any further increase in V will cause a transition to the intermediate state at point A on Fig. 4. If V is then decreased the device will remain in the low impedance state till I_{min} is reached. Any further decrease in V will cause a transition back to the high impedance state at point C of Fig. 4, where $V_{EC} > V_{in}$. On the other hand, if the source voltage is increased when the device is in the intermediate impedance state, the current will increase until I_{max} is obtained at point D in Fig. 4. Any further increase in V will result in a transition to the low impedance state at point E of Fig. 4,

where $V_{EC} < V_{in}$. To bring the diode out of the low impedance state the source voltage V must be lowered until the current flowing through the device is just below I_S. The device will then make a transition to the high impedance state at point G of Fig. 4.

Even though a device does have an intermediate impedance state, its existence may not be apparent in all experiments. Consider the choice of a load resistance $R_L = R_{L2}$, where

$$R_{L2} \lesssim \frac{V_{TH} - V_{in}}{I_{max}} \quad . \tag{5}$$

For such a value of R_{L2} the load line which crosses the device's I-V curve at $I = I_{TH}$ and $V = V_{TH}$ will not intersect the I-V characteristics of the intermediate impedance state. As shown in Fig. 4, any increase in V beyond the point where $V_{EC} = V_{TH}$, will result in a direct transition to the low impedance state at point H of Fig. 4.

In the above discussion it was tacitly assumed that the device was not illuminated. Three changes occur in the device's I-V characteristics when intrinsic radiation is applied to the device: A reduction in V_{TH}, an increase in current carried in the high impedance state, and for many devices, a decrease in I_S. With proper adjustment of bias supply voltage and load resistance, these latter devices can be made to undergo a nonlatching transition to the low impedance state if the transition is triggered by low light levels. Except for this special situation, however, if the threshold voltage V_{TH} is changed from $V_{TH} > V_{EC}$ to $V_{TH}' < V_{EC}$ by optical excitation, then the transition to a lower impedance is generally a latching transition for diodes.

If the load resistance of a particular diode is low enough to satisfy the inequality of Eq. (5), the device may nevertheless be brought to the intermediate impedance state through optical excitation, even though this state

is not accessible in the dark. This is possible because the load line which intersects the optically reduced V_{TH} can also intersect the intermediate impedance state.

Two experiments were performed which supply some quantitative information on the optical suppression of V_{TH}. The devices chosen for this experiment had 300 Å of highly conductive silicon-rich silicon nitride as the insulator and the 6 μm deep junctions were formed by epitaxial growth. The devices were scribed into square chips 5×10^{-2} cm on a side which defined their emitter junction areas, and their opaque circular collector contacts had a 2.5×10^{-2} cm diameter. Under intense tungsten lamp illumination (about 1500 ft. candles) the dark threshold voltage was reduced from 15 V to 7.5 V. With weaker fluorescent light illumination ($\approx$ 35 ft. candles) the threshold voltage was reduced by 0.5 V.

The sensitivity of V_{TH} to light supports the basic model of device operation. Clearly, the creation of electron-hole pairs by optical excitation will aid the development of an inversion layer at lower collector-emitter voltages.

D. Negative Resistance and Uniformity of Conduction

The curves of Figs. 3 and 4 do not explicitly show that a well-defined and continuous characteristic exists between V_{TH} and the low (or intermediate) impedance state. This differential negative resistance (DNR) portion of the I-V characteristic can be traced with direct current if a sufficiently high value of load resistance R_L

$$R_L > \frac{V_{TH} - V_S}{I_S - I_{TH}} \tag{6}$$

is used. Depending upon the reactance in the external circuit, oscillation from several kHz to several tens of MHz has been observed if the load line crosses only the DNR portion of the I-V characteristics as is required by the inequality

of Eq. (6). The ICS therefore is a "negative resistance device without memory" rather than a "switching device without memory" according to the classification of Fritzsche and Ovshinsky [13].

Different runs of ICS's have shown both uniform and nonuniform conduction across the collector region when biased in their low impedance state. The uniformity of conduction can be inferred from experiments in which the sustaining current I_S is measured after consecutive reduction of the same collector area by etching. Devices which show an I_S which is reduced in proportion to area are often structures which have a high sheet resistance ($> 10^3$ Ω per square) of their base region and whose V_{TH} is not greatly sensitive to temperature (Sec. IV). Devices which have the lowest observed values of I_S nearly always have uniform or nearly uniform conduction. In order to observe an I_S that is proportional to area, careful etching (smooth new perimeter and complete removal of unwanted collector metal) must be performed in defining the collector metallization because the most commonly observed nonuniform current distribution is a greater current density which flows near the perimeter of a collector metallization.

Certain runs of devices clearly evidence an extremely nonuniform conduction in their low impedance state. This can be demonstrated if the collector of such a device is divided in half by etching. If, as is sometimes observed, one half of the device has the same I_S and V_{TH} as the original device, the other half will invariably show a higher V_{TH} with generally a different value of I_S. Nonuniform conduction in the low impedance state is not completely unexpected for these structures since they have a current controlled DNR. The region with the lowest value of V_{TH} will conduct first. Furthermore, the temperature of this region will be raised with respect to that of the rest of the device, and therefore the lower V_{TH} region will tend to remain conducting since the V_{TH} will be lowered further as described in Sec. IV. Note that this argument falls short of demanding filamentary conduction since the insulator does

not possess a bulk DNR [14]. Lateral voltage drops produced by internal base resistance and collector sheet resistance will tend to provide for more uniform breakdown, as will the presumably uniform injection of minority carriers from the emitter.

Even the most nonuniformly conducting devices could be cycled between their low and high impedance states more than 10^{11} times (the highest number attempted) without damage. Examining devices for nonuniform temperature distribution by coating the surface of the wafer with a temperature-sensitive liquid crystal film* revealed that all devices conduct extremely uniformly at higher current densities ($\gtrsim$ 50 A/cm^2), even if their conduction at low current was localized. The liquid crystal experiments also confirmed that a uniform temperature distribution existed across the collectors of devices even at low currents if the devices were of the type whose I_S was proportional to area.

IV. TEMPERATURE DEPENDENCE OF V_{TH}

All ICS devices show a decrease in V_{TH} if the ambient temperature T is raised sufficiently. Certain ICS devices have an extremely sensitive dependence of V_{TH} upon T ($dV_{TH}/dT \approx -1$ V/°C) over certain temperature ranges [2], [15]; other ICS devices have a threshold voltage nearly independent of temperature below 200°C [4], [16]. The structural variations responsible for this divergent behavior will be described.

A. Effect of Conducting "Insulator" Material

The choice of insulator material can affect dV_{TH}/dT. Figure 6 displays $V_{TH}(T)$ for three different device structures. Two of these devices had identical semiconductor structures but differed only in the composition of their insulator layer. A marked temperature dependence of V_{TH} is observed for

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* Cholesteric liquid crystal kit obtained from Visual Products Division 3M Company, Cincinnati, Ohio.

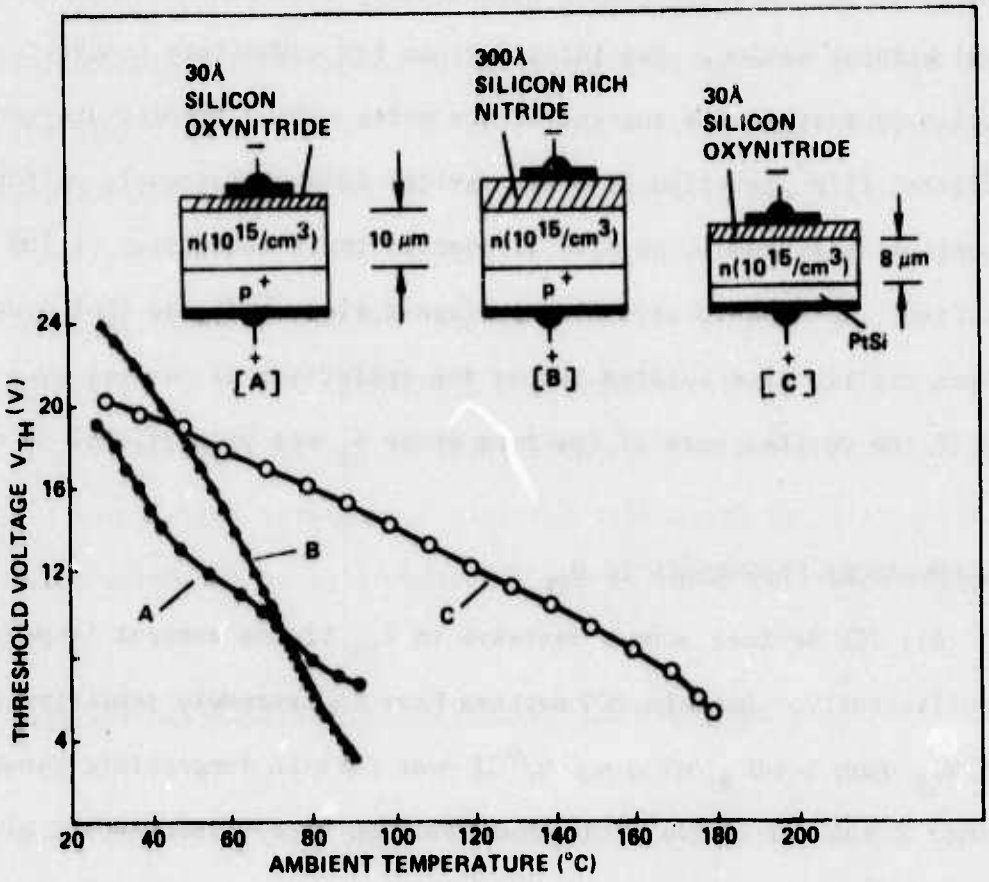

FIG. 6 Diode threshold voltage V_{TH} as a function of ambient temperature for three different ICS structures, all fabricated from the same silicon material which had a relatively lightly doped base region.

both of the devices which have the same semiconductor structure (n/p^+), with the density of the ionized donors equal to $1 \times 10^{15}/cm^3$.

A partial explanation of this behavior involves the different temperature dependences of conduction across the p-n junction and the metal-insulator-semiconductor interface. The minority carrier current injected by the junction will have a temperature dependence of the form $\exp[-q(V_g - V)/kT]$, where V_g is the silicon bandgap voltage and V is the forward voltage. All of the silicon nitrides investigated as ICS insulators have been found to have a relationship between current I and voltage V of the form

$$I = I_o \exp\{q/kT][-\varphi_t + \alpha \sqrt{V}]\} \tag{7}$$

for current densities which include I_{TH} and I_S [2]. Here I_o and α are material constants and φ_t is a trap or barrier height. For the 30 Å silicon oxynitride $\varphi_t \approx 0.65$ eV and for the 300 Å silicon-rich nitride $\varphi_t \approx 0.48$ eV.

The effect of this different temperature dependence of conductivity upon ICS device properties can be pictured in the following manner. Suppose an ICS device is biased just below V_{TH}. In such a situation the minority carriers injected into the base region arrive at the silicon-insulator interface at a rate which is just insufficient to permit a strong inversion layer to form. If the temperature is increased, an inversion layer can form even though the voltage is not increased because the junction's temperature dependence of conductivity is greater than that of the insulator ($V_g > \varphi_t$). Thus, even though the insulator can pass more current at a higher temperature, an inversion layer will form (causing the creation of the low impedance state) because the junction will inject minority carriers toward the insulator at an even higher rate.

This explanation of the temperature dependence of V_{TH} is, however, incomplete because the relations expressed by Eq. (7) were measured under

conditions of accumulation rather than depletion and inversion, and, therefore, do not necessarily express the conduction across the insulator of the majority and minority carriers of the base region individually. The explanation therefore admits neither the possibility of a generalized multiplication at the insulator-semiconductor interface (a specific example of which was discussed by Green and Shewchun [17] for thin SiO_2 layers which conduct by tunneling) nor a rapid change in the ratio of electron-to-hole currents as an incipient inversion layer develops. The latter possibility could occur because of a change in the population of interface states with inversion. The importance of interface states in conduction through metal-insulator-semiconductor structures has been discussed by Card and Rhoderick [18], for example. The data of Fig. 6 do, however, indicate a more sensitive dependence of V_{TH} upon T for the insulator with the smaller φ_t and additional experiments on different silicon nitrides confirm this simple explanation [19].

B. Devices With Barrier Emitters

The inversion-controlled conduction phenomenon has been observed in M/I/n/M structures which have a Schottky-barrier contact to the n-type base as a metal emitter [16]. A Schottky-barrier contact can inject minority carriers into silicon, especially at high current biases [20]. Specific use of this injection mechanism is made in MSM and BARITT diodes [21], [22].

The temperature dependence of the threshold voltage of an ICS device with a PtSi Schottky-barrier emitter is shown in Fig. 6. The metal-conducting insulator region of this device and the doping of its n-type base were identical to that of the metal/silicon oxynitride/n/p^+ device whose temperature dependence of V_{TH} is also shown in Fig. 6. Following the deposition of the silicon oxynitride and the collector metallization, the wafer was divided in half. One half had its p^+ substrate removed by chemical polishing; the final

thickness of the part of the wafer was 8 μm, while the original thickness of the n-epitaxial layer was 10 μm. After the half of the wafer had been thinned and sputter etched, Pt was deposited on its back surface. The Pt was reacted at 400°C to form PtSi. The other half of the wafer, which still had its p^+ substrate, was subjected to the same heat cycle in order to ensure that both the p^+ and PtSi emitter devices had the same annealing of their silicon oxynitride insulator layers in contact with the molybdenum collector metallization. The observed temperature variation of V_{TH} of the PtSi emitter device is significantly smaller than that of the p^+ emitter. This behavior is generally observed for Schottky-barrier emitters, although the data of Fig. 6 represent the only case in which great care was taken to ensure that the collector's metal and insulator layers and the base doping were identical to a comparison $M/I/n/p^+$ device.

The ratio of electron and hole currents crossing the Schottky barrier will differ from that of a p^+-n junction [20], [21] and therefore a different distribution of voltage between the collector depletion region and the emitter junction or barrier will be obtained at the threshold voltage condition of the two silicon oxynitride devices of Fig. 6. Furthermore, a component of hole current I_p crossing the device may be expected to have a dependence on temperature and voltage across the barrier expressed by

$$I_p = A_p^* T^2 \exp[(-q/kT)(\varphi_p + V_B - V)] \quad ,$$

where A_p^* is the effective Richardson constant for holes, φ_p is the barrier height for holes emitted from the metal into the silicon and V_B is the barrier's built-in voltage [22]. Since $\varphi_p \approx 0.2$ V for a PtSi-Si barrier and $V_B \approx 0.8$ V, it may be expected that the temperature dependence of the PtSi emitter will be less than that of junction emitter where $V_g \approx 1.15$ V, in agreement with the data of Fig. 6.

C. Devices With Heavily Doped Bases

If connections are made only to the collector and base terminals, it is possible to determine the avalanche breakdown voltage V_A of the collector from I-V characteristics and the punch-through voltage V_p of the collector depletion layer to the emitter from C-V characteristics (if $V_p < V_A$). (Inversion will not occur if the emitter terminal is left open [6].) All the devices described previously had $V_p < V_A$. A quite different behavior of $V_{TH}(T)$ is observed if $V_A < V_p$ [4], [15].

Devices with $V_A < V_p$ can be fabricated by either using more heavily doped epitaxial layers (or thicker epitaxial layers) or alternately by producing the base layer by diffusion. Figure 7 presents the variation of V_{TH} as a function of temperature for three different semiconductor structures. The curve which shows the smallest variation in V_{TH} with I is a device produced by diffusion of boron into a n-epitaxial layer grown on an n^+ substrate. The sheet resistance of the diffused p-type layer was approximately 100 ohms per square (its junction depth was 2.5 μm). The insulator layer of this device was produced in a manner novel for ICS devices: a silicon-rich nitride was deposited after the diffusion and then it was converted to a silicon oxynitride layer by annealing in dry oxygen for an hour at 1150°C [23], [24].

The diffused device with the greater dependence of V_{TH} upon T had an insulator layer of 30 Å of silicon oxynitride formed by a procedure which is identical to that used to form the silicon oxynitride devices whose $V_{TH}(T)$ curves were displayed in Fig. 6. The diffused p region of this device had a sheet resistance of $\approx 10^3$ ohms per square.

The third device, whose $V_{TH}(T)$ is displayed as a curve in Fig. 7, was fabricated from an epitaxially grown junction rather than a diffused junction. The doping density of the epitaxial base region, as determined from

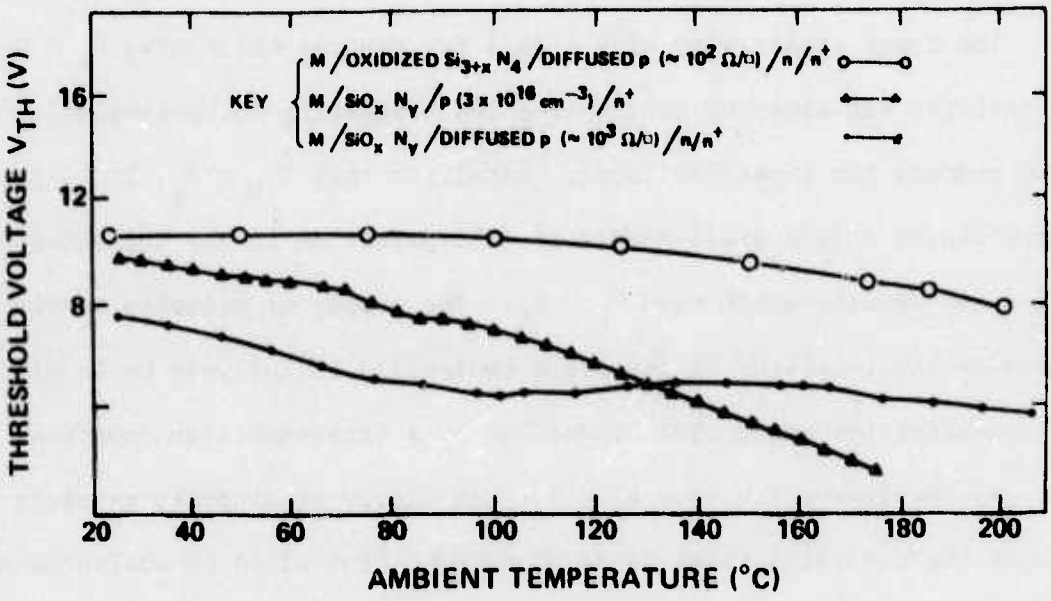

FIG. 7 Diode threshold voltage V_{TH} as a function of ambient temperature for three different ICS structures which had relatively heavily doped base regions.

C-V measurements, was 3×10^{16} cm^{-3}, which is significantly higher than the 1×10^{15} cm^{-3} used in the devices of Fig. 6. The avalanche breakdown voltage of the base layer of this device was determined to be 24 V from measurements on the breakdown voltage of the collector-base terminals. At this voltage a surface depletion layer width of ≈ 1 μm was obtained, which was significantly less than the base layer width of 4 μm. The insulator used to fabricate this device was again the 30 Å of CVD silicon oxynitride used in many of the previously discussed devices. The temperature dependence of V_{TH} upon T is significantly reduced for this device with the more heavily doped base compared to the devices of Fig. 6.

The lower sensitivity of V_{TH} to T for devices which have $V_A < V_p$ can be qualitatively explained by considering the triggering mechanisms which initially produce the inversion layer. Recalling that $V_{TH} < V_p$, it is clear that there can be only a small amount of multiplication in the collector depletion layer for devices which have $V_p < V_A$. The supply of minority carriers which produce the inversion is therefore controlled exclusively by an extremely temperature-sensitive mechansim: injection by a forward-biased junction.

For devices which have $V_A < V_p$, the supply of minority carriers which can trigger the inversion is at least partially controlled by avalanche multiplication. The ionization coefficients will decrease with increasing temperature [25], thereby tending to increase V_{TH} with increasing temperature. An increase of V_{TH} with T is not usually observed, however, since the triggering of the low impedance is also partially determined by injection of minority carriers into the surface depletion zone from the emitter junction, and this latter process will increase with temperature. The lower temperature sensitivity of the change in V_{TH} with T for devices with heavily doped base regions is readily explained by the above considerations, however. Finally, it should be emphasized that even though avalanche multiplication helps to initiate the low impedance state for devices with heavily doped bases, the low impedance state is maintained solely by emitter injection since V_s is too low to permit significant multiplication.

V. SUMMARY AND CONCLUSIONS

A description of the important steady-state characteristics of the two-terminal inversion-controlled switch has been presented. The generality of the appearance of bistable impedance states in metal/conducting "insulator"/semiconductor-junction (barrier) structures has been emphasized. A wide variety of structural variations has been discussed; in particular, the choice of insulator material is not critical for observation of the phenomenon. All insulator materials used to fabricate these structures have resulted in the inversion-controlled conduction phenomenon being obtained if the insulator layer was of appropriate thickness.

Without being stressed to the point of permanent change or damage, an ICS can conduct direct current more than 10^3 times greater than would be necessary for operation of the device in digital circuits. The device is therefore in no sense fragile even though some structural variations have relatively thin insulator layers. Other variations of the devices, particularly those using CVD polysilicon as the insulator layers, need not have any layer thinner than 0.2 - 1.0 μm.

ICS devices potentially could be used in a variety of applications. If a device structure is chosen which has a temperature-sensitive threshold voltage, then the device could be used as a temperature sensor or an alarm; devices with temperature-insensitive threshold voltages could be used as light-sensitive alarms, in special fusing applications or in digital applications because of their binary impedance states. Among these are cross-bar switching matrices, and controlled rectifiers, as well as memory and logic applications. The latter two will be described in subsequent publications.

VI. ACKNOWLEDGEMENTS

The authors wish to thank L. W. Currier who skillfully fabricated all the devices described in this paper, and R. Newman for illuminating discussions on the ICS phenomenon.

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APPENDIX B

Steady-State Characteristics of Three terminal Inversion-Controlled Switches*

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ABSTRACT

The direct current-voltage (I-V) characteristics of three terminal inversion controlled Switches are described. These devices are layered sequences of metal/conducting "insulator"/semiconductor junction with electrical terminals at the metal and both sides of the junction. If a bias is applied between the metal and the far side of the junction, in the sense which tends to deplete the surface and forward bias the junction, the device shows bistable impedance states similar to the current-voltage characteristics of a silicon-controlled rectifier. The intermediate terminal which contacts the semiconductor region between the insulator and the junction, can be used, in proper circuit and biasing arrangements, to switch the device both into and out of its low impedance state without varying the voltage supplied to the outer terminals of the device and a series-connected resistor. The I-V characteristics of these three terminal devices support the inversion-controlled conduction model of device behavior which permits high conductivity of the device only when inversion of the semiconductor surface occurs. The high and low impedance states and the pulses required to induce transitions between states are contained entirely within the "active" bias configuration for these devices, which is defined by analogy with the active bias region of conventional bipolar transistors.

I. INTRODUCTION

The current-voltage (I-V) characteristics of a wide variety of structural variations of two terminal inversion-controlled switches (ICS) have been described in the preceding paper [1] (hereafter called I). This paper contains a description of the steady-state properties of the more interesting and important three-terminal versions of these devices. Like the two terminal devices of I, the three terminal devices are a layered sequence of metal/conducting "insulator"/n-type silicon/p-type silicon or metal/conducting "insulator"/p-type silicon/n-type silicon. While the two terminal devices had electrical contact made only to the metal and the far side of the p-n junction, the three terminal devices which are the subject of this paper also have electrical contact to the semiconductor region between the insulator and the junction [2]-[4].

Two typical device structures which have been studied are diagrammed in Fig. 1 for the M/I/p/n type of structure. The "emitter," "base" and "collector" regions are defined by analogy with the functions performed by the corresponding parts of a conventional bipolar transistor [2]. The "emitter" of an ICS injects minority carriers into the "base" region. Like the collector of a bipolar transistor, the "collector" of an ICS has a depletion region which sweeps up minority carriers from the base. It is important to note that the base electrode does not make contact with the collector's depletion zone. The base terminal, therefore, functions largely as an independent control of the emitter-base potential. Prooosed circuit symbols for the ICS transistor have been introduced in I.

This paper is descriptive and emphasizes the evidence provided by the behavior of the three terminal devices for the inversion-controlled conduction model of device behavior [5]. This model associates the low and high impedance states with the presence or absence, respectively, of an inversion layer at the semiconductor surface [1], [2], [5].

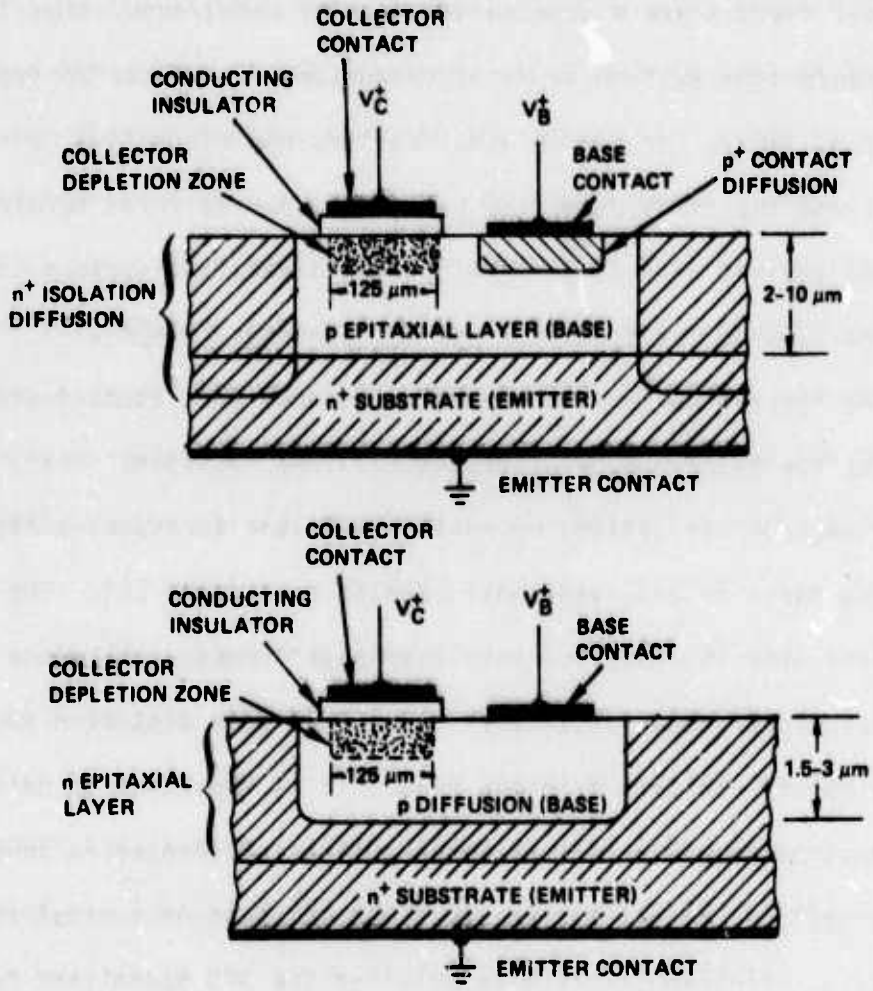

FIG. 1 Cross sectional views of two typical three terminal ICS structures illustrated for M/I/p/n device.

Top: Epitaxially grown junction.

Bottom: Diffused junction.

The full range of behavior of three terminal ICS I-V characteristics is presented. The grounded emitter characteristics are described in Sec. II, including for the first time a description of the capability of the third intermediate (base) terminal to switch a device out of its low impedance state. The grounded-base characteristics of the ICS, which have not previously been discussed, are presented in Sec. III. The switching characteristics of ICS devices are mentioned in Sec. IV. Section V summarizes the paper and includes a discussion of possible applications.

II. GROUNDED EMITTER I-V CHARACTERISTICS

A. Reduction of V_{TH} by Base Current

The three terminal I-V characteristics of devices which have electrical connection to each of the emitter, base, and collector regions have already been described for one particular device structure [2]. The basic observation is that the collector threshold voltage V_{TH} measured with respect to the emitter is lowered when the emitter-base junction is forward biased by means of the base contact. (The threshold voltage V_{TH}, which is the highest voltage which can be applied to an ICS device, has been previously defined [1]-[3], [5].) This is in agreement with the inversion controlled conduction model of device behavior: Increasing the forward bias of the junction will increase the minority-carrier concentration in the base, thereby limiting the capability of the insulator to discharge the incipient inversion layer. Independently increasing the junction's rate of minority-carrier injection into the base by using three terminal devices should therefore lower the emitter-collector threshold voltage V_{TH} for transition into the low impedance state.

The lowering of the threshold voltage by a forward emitter junction current is found in all three terminal structures. The device structure described in Ref. [2], which was a M/polysilicon/p/n^+ structure, was exceptional with

respect to the extreme sensitivity of its V_{TH} to the base current I_B. These devices had $V_{TH}(I_B)$ given by

$$V_{TH}(I_B) \approx 9 - (3.6 \times 10^5\ \Omega)I_B, \quad \text{for } I_B \leq 20\ \mu A \quad , \tag{1}$$

where $V_{TH}(I_B = 0) = 9$ V was the threshold voltage of the equivalent diode structure with the base terminal left unconnected [2]. Other structures, including $M/SiO_2/n/p^+$ devices, have shown a similar sensitive linear suppression of V_{TH} with increasing I_B. For example, $V_{TH}(I_B)$ obtained with a 35 Å SiO_2 layer device whose C-V characteristics were displayed in Fig. 5 of I, is

$$V_{TH}(I_B) = 13.4 - (3.7 \times 10^5\ \Omega)\ I_B, \quad \text{for } I_B \leq 25\ \mu A \quad . \tag{2}$$

A more typical relationship between V_{TH} and I_B is shown in Fig. 2. These data were obtained from a M/silicon-rich, silicon nitride/p/n^+ device. Besides having a significantly smaller value of $|dV_{TH}/dI_B|$, these data also show that $|dV_{TH}/dI_B|$ decreases with increasing I_B, unlike the linear relationship of Eqs. (1) and (2). The devices from which these data were obtained had the same area (1.27×10^{-4} cm^2) as the devices whose behavior is described by Eqs. (1) and (2).

The application of a base current to the device usually has no effect upon the characteristics of the low impedance state other than a slight increase in V_S, which is usually much less than 0.1 V. (The sustaining voltage V_S is the minimum voltage of the low impedance state and has been described in I.) The introduction of a circuit connection between emitter and base can have an important effect upon the low impedance state, however, and this effect will be described in the next section.

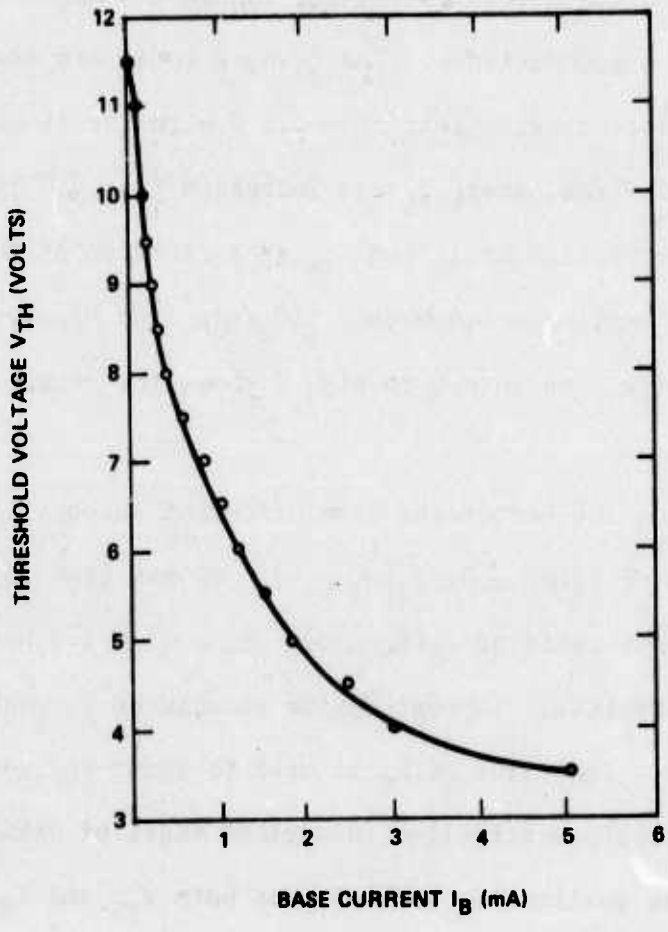

FIG. 2 Variation of grounded emitter threshold voltage V_{TH} as a function of applied base current I_B for a metal-silicon-rich, silicon nitride-p-n^+ device.

B. Effects of Emitter-Base Shunt Resistance

Three changes in I-V characteristics occur where a shunt resistance R_S is placed between the emitter and base terminals of an ICS device. The sustaining current I_s (the minimum current of the low impedance state as discussed in detail in I.), the sustaining voltage V_{in} of the intermediate state, as defined in I., and the threshold voltage V_{TH} of the high impedance state, are increased by a shunt conductance. The changes in V_S are small, usually not exceeding 10% and often being less than 0.1 V with the single exception of certain $M/SiO_2/n/p^+$ devices, where V_S was increased from 2.0 to 4.5 V. Figures 3 and 4 illustrate the variation in I_S and V_{TH} as a function of the emitter-base shunt resistance R_S for devices which have $M/SiO_2/n/p^+$ and M/polysilicon/p/n^+ structures, respectively. The insert to Fig. 3 shows the circuit used to obtain the data.

Different ICS structures show different changes in I_S and V_{TH} with R_S. The maximum ratio of $I_S(R_S \approx 0)/I_S(R_S \approx \infty) = 30$ has been observed for $M/SiO_2/n/p^+$ devices; the minimum ratio of $I_S(R_S \approx 0)/I_S R_S \approx \infty) = 1.3$ has been observed for $M/SiO_xN_y/p^+/n/n^+$ devices. In most device structures I_S changes by a factor of three to six when a low value of R_S is used to shunt the emitter and base.

The inversion-controlled conduction model of device behavior is in agreement with the qualitative variation of both V_{TH} and I_S with R_S. Shunting of the emitter junction requires that a smaller fraction of the current drawn across the collector results from injection of majority carriers of the emitter into the base. If a device is in the high impedance state a higher voltage is required to develop an incipient inversion layer at the semiconductor-insulator interface. If a device is in the low impedance state, a higher current must be used to maintain the inversion layer.

There are also practical applications for the variations of I_S with R_S In contrast with the behavior of diodes, the dependence of I_S upon R_S provides a

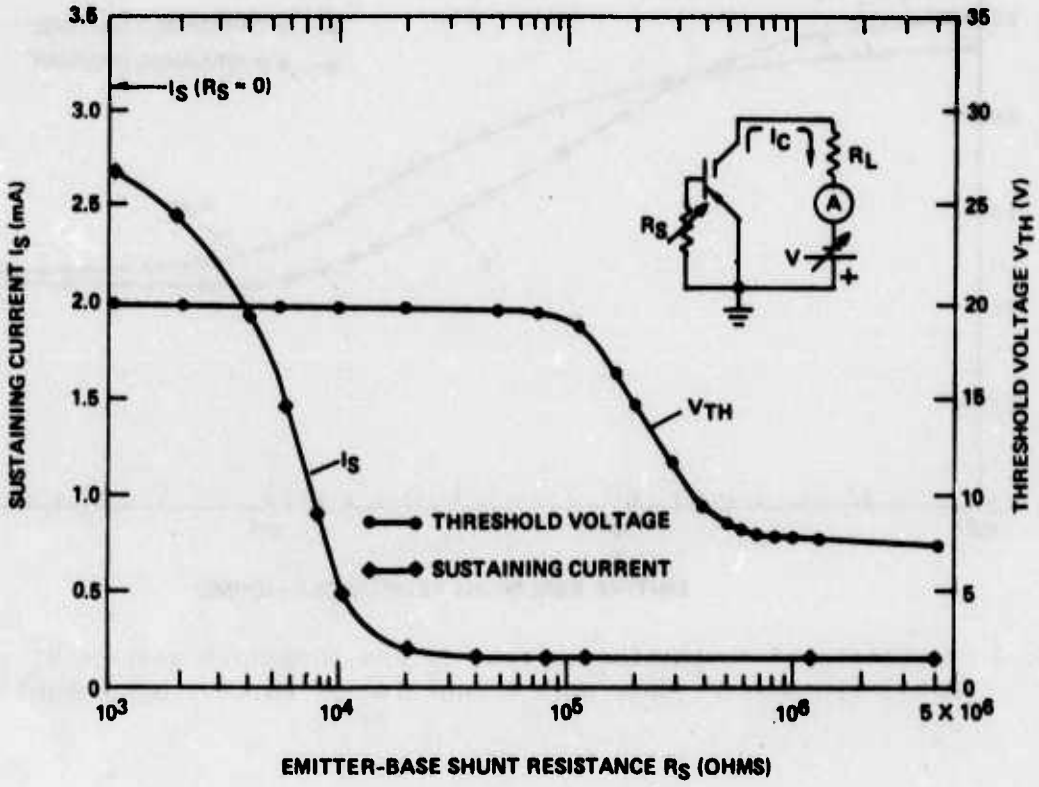

FIG. 3 Variation of sustaining current I_S and threshold voltage V_{TH} of a metal-SiO_2-n-p^+ device as a function of emitter-base shunt resistance R_S.

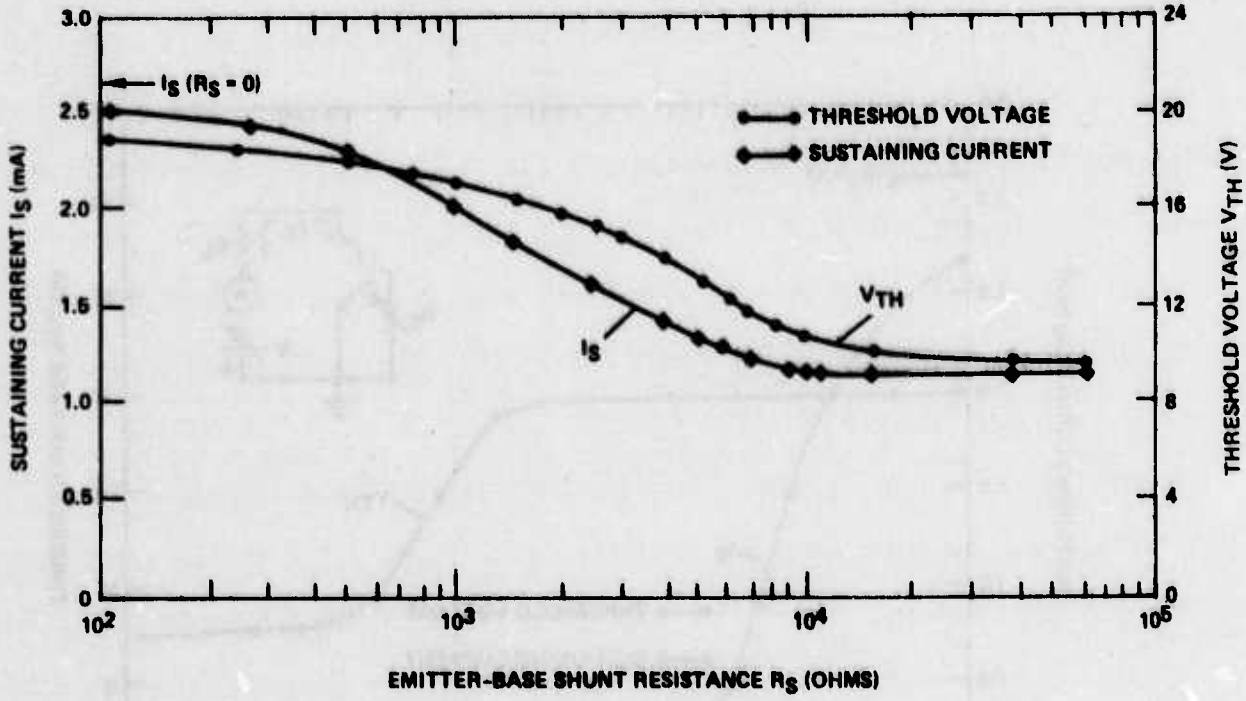

FIG. 4 Variation of sustaining current I_S and threshold voltage V_{TH} of a metal-SiO_xN_y-p-n^+ device as a function of emitter-base shunt resistance R_S.

for switching a device out of its low impedance state without lowering the collector voltage. The only requirement is that the collector current I_c (determined by R_L and V, shown in the insert to Fig. 5) be not greater than $I_S(R_S \approx 0)$ in the low impedance state. As shown in Fig. 5, a transition from point A in the low impedance state to point B in the high impedance state is possible without reducing I_c to $I_S(R_S \approx \infty)$. The variable shunt resistance R_S has been provided by variable resistors, FET's or other ICS devices.

C. Latching vs Nonlatching transitions

If a dc voltage is applied to the series combination of the device and a load resistor and V_{TH} is reduced by application of base current, then the device will generally remain in its low impedance state even after the base current is removed. Such a transition to the low impedance state is called a latching transition. The inclusion of an emitter-base shunt resistance, as shown in the insert to Fig. 5, permits the possibility of nonlatching transitions in which the device returns to the low impedance state following the removal of the base current pulse.

In order to observe nonlatching transitions, the collector supply voltage V and the collector load resistance R_L must be chosen so that the interaction of the load line with the low impedance characteristic occurs at a current less than $I_S(R_S)$. The application of base current will permit the device to trace out a low impedance state characteristic to lower values of current and this characteristic is essentially identical to that which could be obtained with a higher value of R_S but without the base current. A possible nonlatching transition could therefore be from B → A → B of Fig. 5, with the device residing at point B only for the duration of (a large enough) base current.

The distinction between latching and nonlatching transitions has important practical applications. Circuits which exclusively permit latching transitions to occur are useful as memory elements; circuits which exclusively

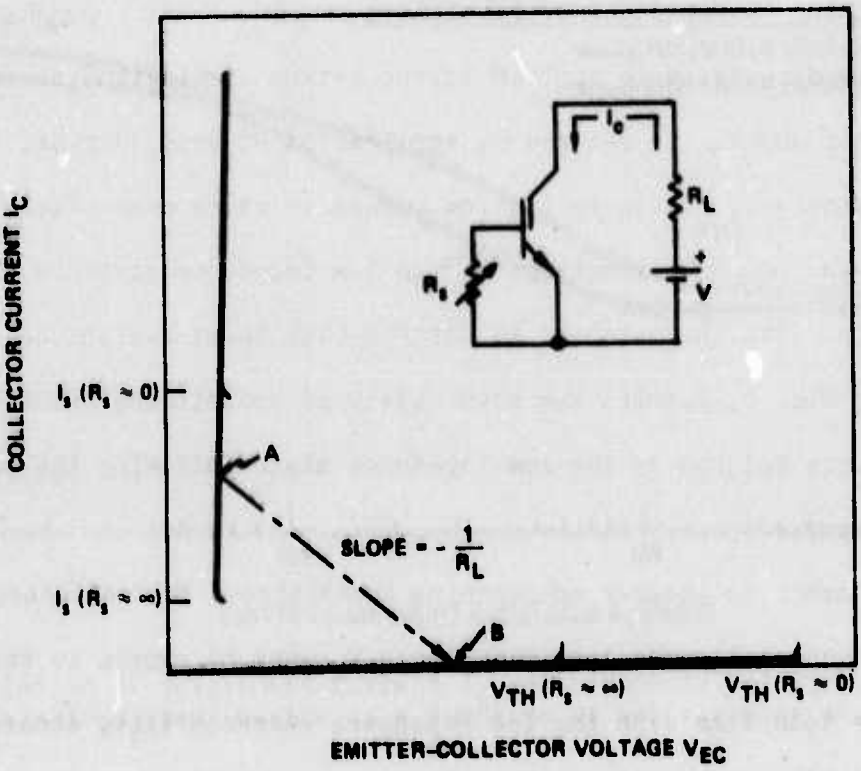

FIG. 5 I-V characteristics of grounded-emitter ICS device for large and small values of base shunt resistance R_S. Transition from point A to point B is possible by only lowering R_S (without changing V or R_L).

permit nonlatching transitions to occur can be used to perform logic functions.

III. GROUNDED BASE I-V CHARACTERISTICS

A. Effect of Emitter-Base Shunt Resistance

If an ICS is connected in a grounded base configuration, then no transition to the low impedance state can take place unless provision is also made in the circuit to supply current to the emitter terminal. Although collector breakdown can be observed with an open emitter, switch-back to a lower voltage state cannot be observed. Similarly, a device fabricated with no p-n junction and with contact to the semiconductor by means of a noninjecting contact will not show a low voltage state, even if the insulator and collector contact are identical to a fully functional ICS device. The necessity of having a nonzero emitter current in order to produce the low voltage state is in obvious agreement with the inversion-controlled conduction model of the device behavior.

One method of providing a finite emitter current is to provide a shunting resistance R_S between emitter and base terminal, as shown in Fig. 6(a). The open-base grounded emitter I-V characteristics of a molybdenum/SiO_xN_y/p^+/n/n^+ structure are shown in Fig. 6(b). The grounded base I-V characteristics of the same device are presented in Fig. 6(c). These latter characteristics are shown for four different values of emitter-base shunt resistance: $R_S \approx 0$, 100, 200 and 400 Ω. For small currents the differential resistance in the low impedance state is slightly less than the value of R_S used to generate the particular curve. The variation of the slope of the I-V characteristic with R_S implies that most of the collector current is drawn through the emitter terminal even in the grounded base configuration, and this is confirmed by direct measurement. The fact that the slope is measurably less than R_S results from a nonzero base current which provides a parallel path to the emitter circuit. For this particular device the base current is between 15 and 25 percent of the collector current,

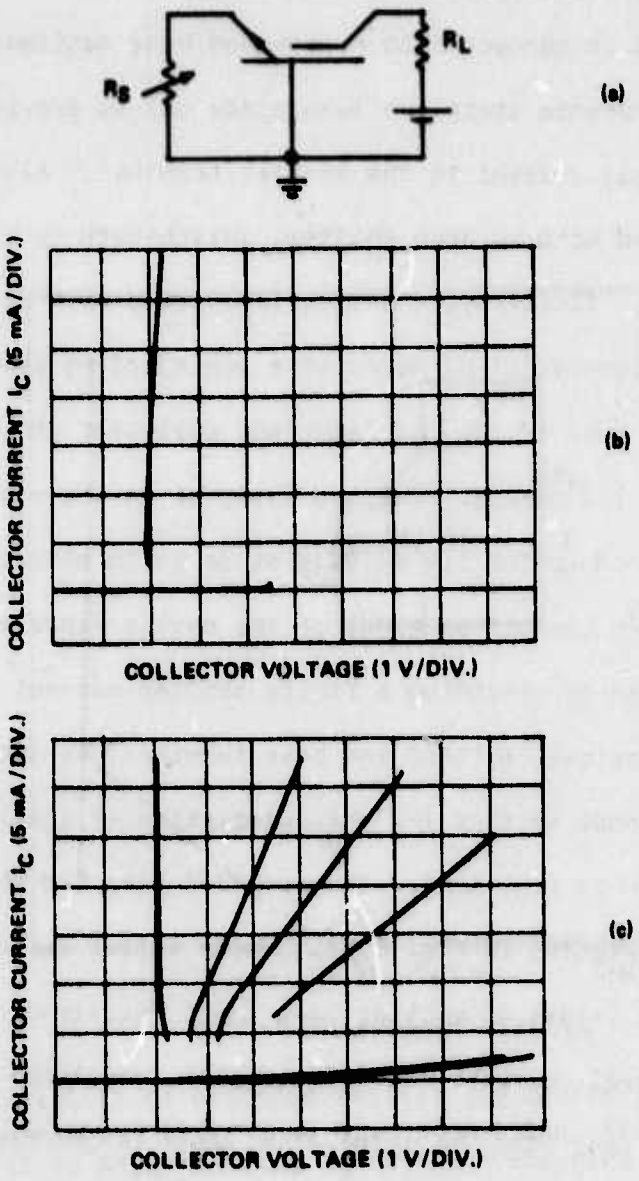

FIG. 6 Grounded base biasing of a metal-SiO_xN_y-p^+-n-n^+ ICS device.

(a) Grounded base circuit.

(b) Grounded-emitter I-V characteristics shown for comparison.

(c) Grounded-base characteristics with $R_S \approx 0$, 100, 200 and 400 ohms.

varying according to collector bias and the values of R_S and R_L. (This particular device has a low emitter efficiency compared to conventional bipolar transistors because the n-type emitter is less heavily doped than the diffused p-type base.)

For values of $R_S \gtrsim 1000\ \Omega$, no transition to the low impedance state occurred for this device. The effect of an emitter-base shunt for grounded base biasing is therefore opposite to that of a shunt resistance applied to a grounded emitter configuration. Lowering the values of R_S always tends to cause a device with grounded emitter to switch out of the low impedance state, whereas raising the level of R_S tends to cause a device with grounded base to switch out of the low impedance state.

The characteristic for the grounded base configuration with $R_S \approx 0$ is identical to that for the grounded emitter configuration with $R_S \approx 0$. Compared to the grounded emitter characteristics shown in Fig. 6(b), V_{TH} has increased to 10 V for $R_S \approx 0$, from $V_{TH} = 4.5$ V. The grounded base threshold voltage is not as sensitive to R_S as the grounded emitter configuration.

When operated in the grounded emitter mode this particular run of devices shows only a slight change in I_S when R_S is varied between infinity (Fig. 6(b)) and zero (Fig. 6(c)). In order to switch the device out of the low impedance state by varying R_S, a fairly precise adjustment of the collector supply voltage would therefore be necessary. On the other hand, the grounded base configuration removes all requirements for precise control of the collector supply voltage.

Figure 7 illustrates how this same device can be removed from the low impedance state by variation of R_S. The data of Fig. 7 were obtained by the following procedure. For each particular value of collector supply voltage chosen, R_S was increased continuously until the device had switched out of the low impedance state. The straight lines traced by this procedure are collector load lines for a 150 Ω collector load resistance. These load lines terminate

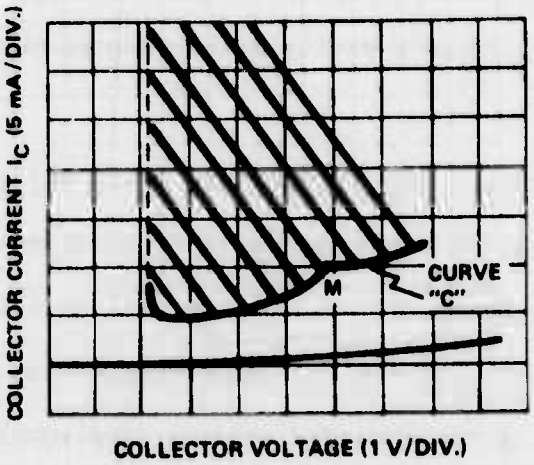

FIG. 7 Grounded base characteristics of same device used in obtaining data of Fig. 6. Straight-line characteristics were produced by a continuous increase of R_S from 10 Ω until device switched out of low impedance state. Dotted line shows low impedance state characteristic when R_S = 10 Ω; the curve C marks the lower limit of the low impedance state.

at the upper left on the I-V characteristic corresponding to R_S = 10 Ω, the smallest value of R_S used in this experiment; they terminate at the lower right at the limit of the low impedance state. The high impedance state's I-V characteristics are also shown in Fig. 7 to emphasize that there is a gap between the lower limit to the current which can be carried in the low impedance state and the current carried in the high impedance state. Collector supply voltages as low as 2.5 V and as high as 12 can be used while still maintaining the capability of switching this device out of the low impedance state without changing any circuit component except R_S.

The curve C shown in Fig. 7 marks the boundary of the low impedance state. The boundary curve is concave up with $|dI/dV|$ at low voltages exceeding dI/dV at higher voltages. In this respect it is typical of most devices. The small sharp maximum M in curve C is peculiar to this run of devices and the particular load resistance used. This feature is a manifestation of an intermediate conductivity state for collector currents just below M.

B. Effect of Emitter Current on I-V Characteristics

If current I_E is supplied to the emitter by the circuit of Fig. 8(a), the device can switch to a low voltage state. If $R_S = \infty$, then this switching is always a nonlatching transition with the device returning to the high impedance state after the switch S is opened. With $R_S = \infty$, the collector current tends to saturate at I_E for low collector voltages. This particular circuit configuration, which involves the application of an emitter current with essentially no external conductance across the emitter-base terminals, is the only one discovered which often results in damage to many types of devices if a large supply voltage is used in the collector circuit. The damage is caused by large current and voltage swings in the collector circuit, since the device often tends to oscillate rather than establish itself in a well-defined low

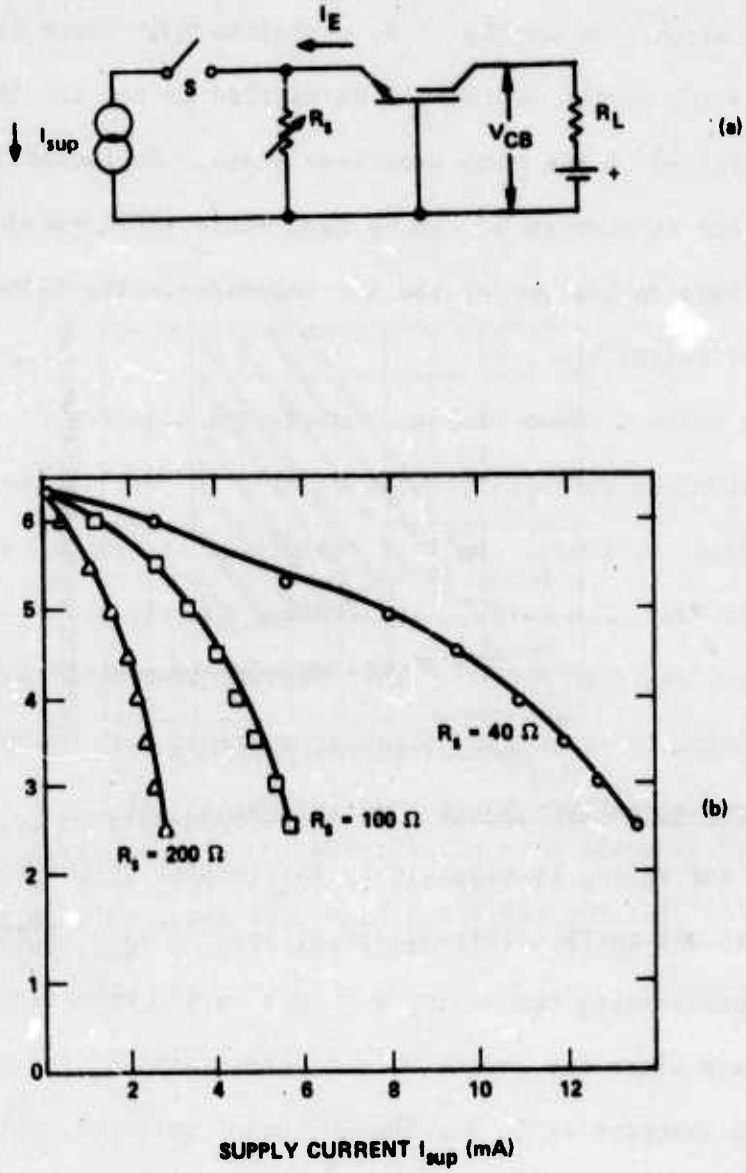

FIG. 8 Effect of emitter$_+$ current on grounded base threshold voltage of a metal-SiO_2-p^+-n-n^+ device.

(a) Circuit used to obtain data.

(b) Variation of base-collector threshold voltage as a function of current I_{sup} supplied to parallel combination of R_S and emitter-base terminals.

voltage state. However, if $R_S \neq \infty$, then safe, repeatable operation occurs.

The collector threshold with grounded base biasing is reduced if any emitter current is supplied. V_{TH} as a function of I_{sup} is presented in Fig. 8 for three different values of R_S for a $M/SiO_2/p/n/n^+$ device. Increasing R_S causes a greater fraction of I_{sup} to enter the device as emitter current, which accounts for the more sensitive suppression of V_{TH} when larger R_S is used. At high values of I_{sup} the observed threshold voltage approaches that for grounded emitter configuration, which was 2.4 V for this device.

IV. SWITCHING BETWEEN STATES

Although a full discussion of the transient behavior of ICS devices is beyond the scope of this paper, several observations are appropriate. First, like conventional bipolar switching transistors, narrow base widths provide for the possibility of more rapid transition between states. Second, the transition time between states is determined for many devices by the $R_L C_C$ time constant where R_L is the collector load resistance and C_C is the total capacitance between the collector terminal and ground. Experiments in which the time constant is purposefully varied have resulted in transition time equaling $R_L C_C$ for both transitions into and out of the low impedance state.

Transitions from high to low impedance states as short as 1 ns ($R_L = 10^3\ \Omega$, $C_C = 1$ pF) have been observed when the device is switched by a fast rising collector voltage. The high-to-low impedance state transition is found to also depend upon dV/dt and the extent of any overvoltage beyond the dc threshold voltage which can be applied in transient conditions. A mode of transition in which the collector current peaks before it attains its steady-state value has been previously described [5]. This mode of transition has not been observed in most devices fabricated since the early experiments described in Ref. 5.

Transitions from the low impedance state to the high impedance state have been studied using a mercury-wetted reed switch to complete a circuit connection which places a 50 Ω resistance between base and grounded emitter. (The capability of an emitter-base shunt resistance to remove a device from the low impedance state has been described in Sec. II. B.) Transition times as low as 3 ns ($R_L \approx 200\ \Omega$; $C_C \approx 15$ pF) have been observed.

V. SUMMARY AND CONCLUSIONS

A description of the important steady-state characteristics of three-terminal inversion-controlled switches has been presented. The behavior of the three terminal devices serves to corroborate the basic model of the device mechanism; the high impedance state is described by deep depletion and the low impedance states by at least the partial development of inversion. The explanation of device behavior therefore involves the language necessary to describe MIS capacitors. However, the total range of device behavior can be usefully modeled by exploiting the analogous structural and functional relationships which the device shares with a conventional bipolar transistor. The third intermediate terminal which provides a connection to the base region of the device is useful for controlling transitions both into and out of the low impedance state.

The discussion of three terminal characteristics of the ICS devices was confined to the case where the device is biased in its "active" region. The active region of ICS devices is defined by analogy with the active bias region of conventional bipolar transistors: the emitter junction is forward biased and the collector is reverse biased. Both the high and low impedance states of the ICS exist within the active bias region. Furthermore, transitions between the high and low impedance states can be obtained without departing from the active region. Of special importance is the fact that the low impedance state does not require saturation (forward bias of the collector) nor does turning off the low impedance state require either reverse bias (cut off of the emitter junction) or

even lowering of the collector supply voltage. These considerations imply that the device is capable of rapid transition out of the low impedance state since the collector is always biased, as it were, in a sense which tends to destroy the low impedance state.

Devices with temperature-insensitive threshold voltages suggest numerous digital applications because of the binary impedance states. Among these are cross-bar switching matrices, controlled rectifiers, as well as memory and logic applications. The presence of the base terminal connection greatly extends the utility of the device since it provides an independent means of turning the device both on and off.

Logic and memory applications have been studied extensively. Logic circuits are possible with simple ICS circuits because, as described in Sec. II of this paper, inclusion of a finite external conductance between emitter and base terminals makes it possible to construct nonlatching circuits, even for the grounded emitter configuration.

The binary states of an individual device suggest that simple memory circuits are possible, and, in fact, small radom-access memory arrays using discrete devices have been operated. These circuits function as static memories with only a single active element per memory site and will be described in subsequent publications. Single bit write, erase, and nondestructive read operattions are possible in these circuits, and the devices can be addressed with ICS or more conventional bipolar logic.

VI. ACKNOWLEDGEMENTS

The authors wish to thank L. W. Currier, who skillfully fabricated all the devices described in this paper, and R. Newman for illuminating discussions on the ICS phenomenon.

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APPENDIX C

Memory Switching in Polycrystalline Silicon Films

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SUMMARY

Nonvolatile memory switching has been observed in polycrystalline silicon layers produced by chemical vapor deposition. Evidence for filamentary conduction is found for devices which are in their low impedance state. Devices have been cycled through high and low impedance states a maximum of 2×10^4 times. Exposure to transient ionizing electron radiation caused the devices to switch to their low impedance state.

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INTRODUCTION

Memory switching, as defined by Fritzshe and Ovshinsky,[1] requires the existence of two impedance states which are stable at zero applied bias. Memory switching has been observed in a wide variety of amorphous materials[2] including evaporated amorphous silicon.[3] It has also been observed in crystalline materials,[4] in GaAs Schottky diodes,[5] and in a variety of heterojunction diodes.[6] The present paper reports observation of memory switching in polycrystalline silicon layers which were prepared by conventional chemical vapor deposition (CVD).

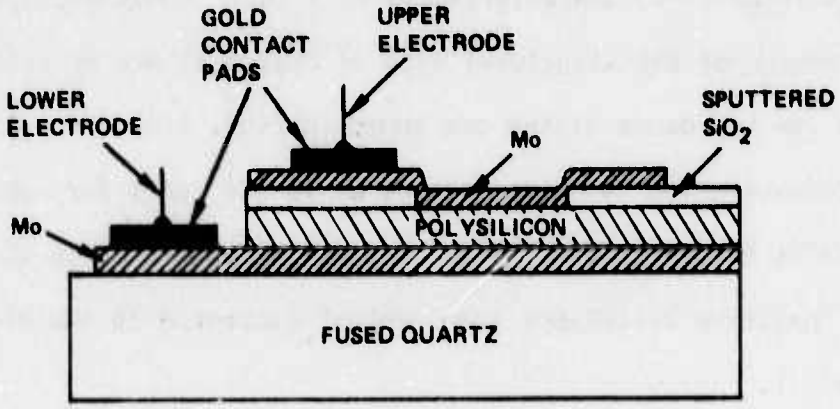
DEVICE STRUCTURES AND PREPARATION

The primary structures investigated are shown in Fig. 1. Thermally oxidized silicon wafers could be substituted for the fused quartz substrate of Fig. 1(a) without affecting device performance.

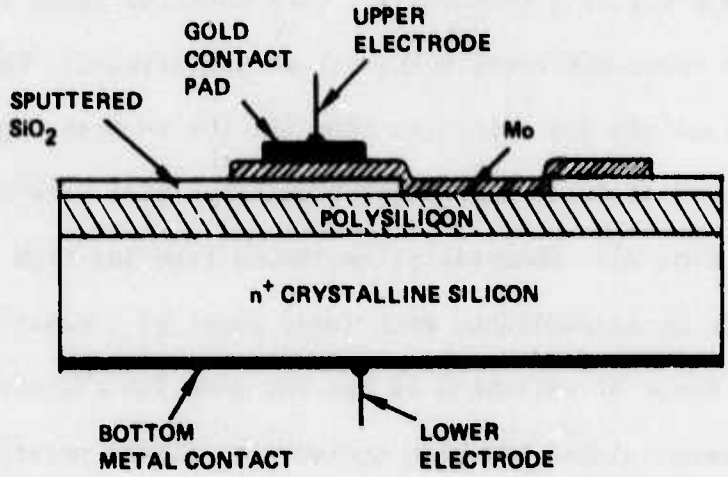
The polycrystalline silicon layers (0.3 - 2 μm thick) were deposited in a cold-wall horizontal reactor by the thermal decomposition of silane using argon or argon-hydrogen mixtures as the carrier gas. The deposition temperatures were 700-800°C, with the temperature held below 720°C for depositions onto molybdenum in order to prevent reactions between the molybdenum and silicon. No *in situ* etching of the silicon substrates was performed prior to deposition in order to form the structure of Fig. 1(b). Thus the polysilicon was deposited over 8-15 Å of nascent SiO_2 formed on the silicon substrate during transfer to the reactor and initial heating of the substrate. For depositing doped silicon layers, phosphine or diborane was introduced into the reactor using a carrier gas that was at least 20% hydrogen. Undoped polysilicon layers were deposited using both pure argon and argon-hydrogen mixtures as the carrier gas.

SWITCHING CHARACTERISTICS

All devices tested showed memory switching and their initial state was one of high resistance. Most devices had a virgin state whose upper limit of



(a)



(b)

FIG. 1 Basic device structures investigated. Note that gold contact pads are not directly above active area of polysilicon.
(a) Molybdenum – polysilicon – molybdenum structure.
(b) Molybdenum – polysilicon – single crystal silicon structure.

voltage was higher than that obtained in all subsequent transitions to the high impedance state after the device had been cycled into its low impedance state. The current-voltage (I-V) characteristics of a Mo – undoped polysilicon (2 μm thick) – Mo device of the structural type of Fig. 1(a) are presented in Fig. 2. The high and low impedance states are shown in Figs. 2(b) and (c), respectively. The high impedance state has a resistance of 10^4-10^5 ohms for applied voltages less than 0.5 V; the ohmic low impedance state's resistance is 50 ohms. The device is a "negative resistance with memory" according to the classification scheme of Ref. 1.

Although these I-V characteristics appear quite symmetric about the origin there is some polarity dependence. (The positive sense of voltage corresponds to the upper electrode being biased positively.) For the majority of devices on most wafers the switching from the low to high impedance state could be accomplished at lower current if a positive bias were used (about 10 mA for the device of Fig. 2). Conversely, switching from the high to low impedance state usually could be accomplished with lower power if a negative bias were used. The "easy" sense of switching is not the same for all devices. However, once switching between states has been cycled with either polarity, an attempt to accomplish the switching with a reversal in polarity always requires larger currents or voltages (typically twice as much) and often will result in permanent damage to the device. Stored at room temperature, the impedance level of a device in either state with no applied bias will change less than 5% over a six-month period.

The I-V characteristics of a Mo – p type polysilicon (2 μm thick) – Mo device are shown in Fig. 3. The virgin state's characteristics, presented in Fig. 3(a), show that this device also evidences threshold switching where the low resistance state does not exist at zero bias, unlike the requirement for memory

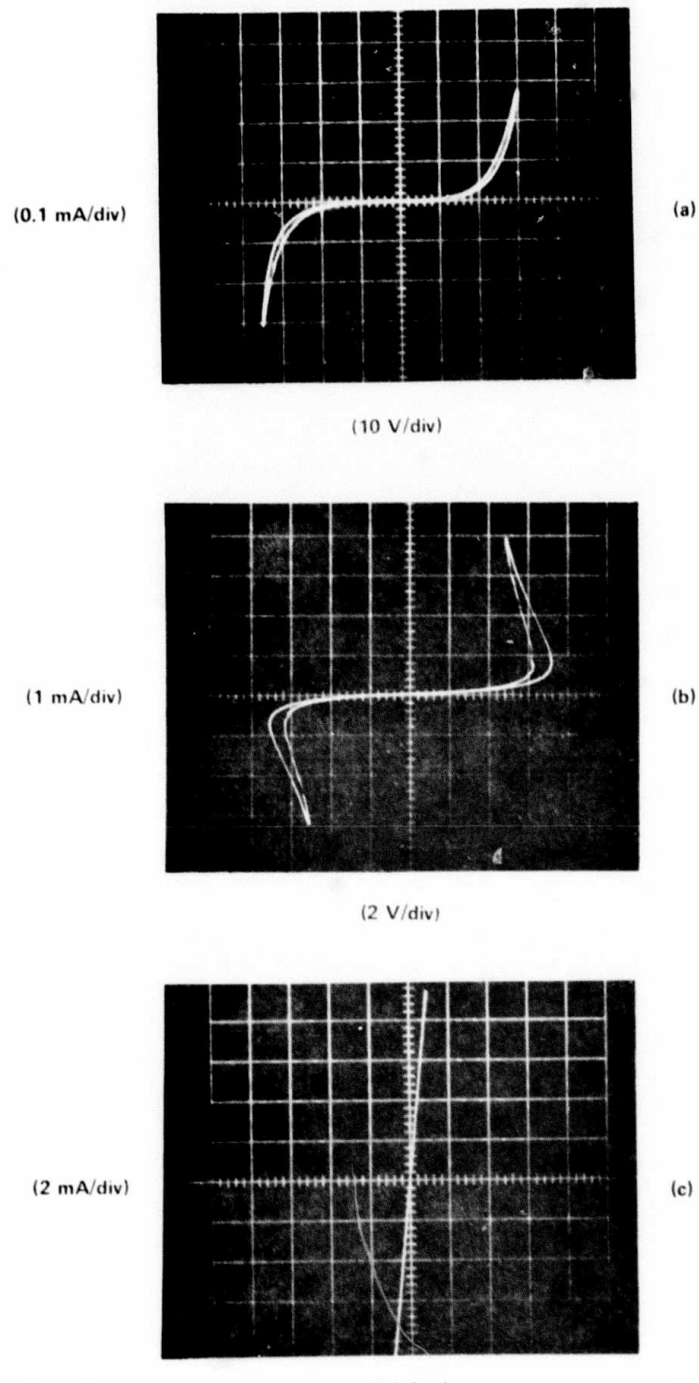
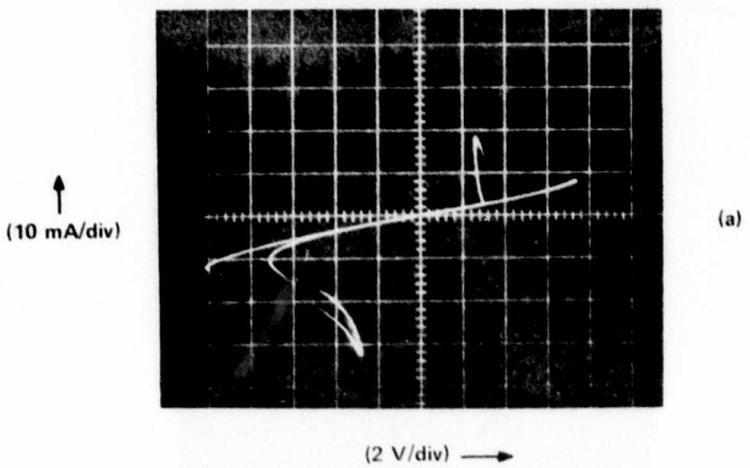


FIG. 2 Current-voltage characteristics of molybdenum – undoped polysilicon – molybdenum device.
(a) Virgin state.
(b) High impedance state.
(c) Low impedance state.



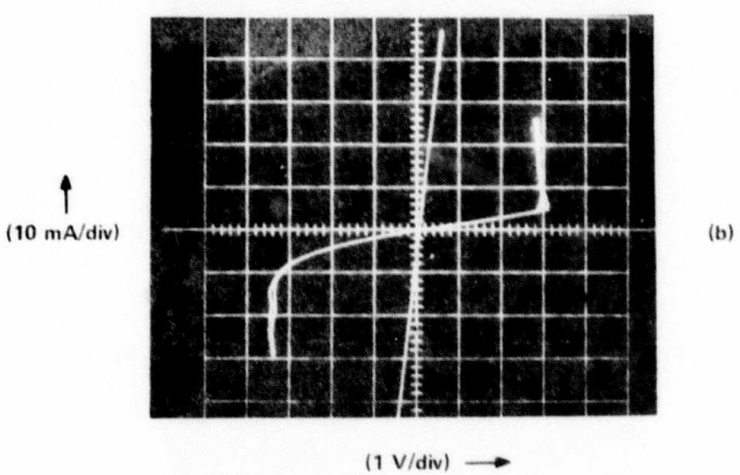


FIG. 3 Current-voltage characteristics of molybdenum – p-type polysilicon – molybdenum device.
(a) Virgin state.
(b) High and low impedance states.

switching.[1] However, threshold switching is usually not observed in these polysilicon devices. The behavior of the polysilicon devices therefore differs from that of amorphous silicon layers described by Feldman and Moorjani.[3] The presence or absence of threshold switching is not correlated with doped or undoped polysilicon layers, or, indeed, with any purposefully controlled property of the layers. It is sometimes observed that not all devices on a single wafer will show threshold switching in their virgin state, even though they may all have similar high and low impedance state characteristics.

The virgin state's characteristics of Fig. 3(a) and the high impedance state's characteristics of Fig. 3(b) do evidence a generally observed property of doped polysilicon devices: the resistances of both the virgin and high impedance states are lower than those obtained with undoped layers. (Both the devices of Figs. 2 and 3 have the same area (1.25×10^{-4} cm^2).) Since the low impedance state's resistance is not greatly affected by doping, the ratio of the resistances in the high and low impedance states is generally smaller for doped layers.

Thicker layers of polysilicon produced by the same procedures but deposited on insulating substrates had resistivities of 100 ohm-cm. If the device had ideal ohmic contacts, then its resistance would be 160 ohms (area = 1.25×10^{-4} cm^2; thickness = 2×10^{-4} cm). The resistance of the device in the high impedance state at low voltage is $\approx$ 600 ohms, suggesting that the contacts are not ohmic. This particular polysilicon layer was deposited at 700°C, and at this temperature the first 0.1-0.2 μm of material deposited may be in an amorphous rather than a crystalline form,[7] perhaps accounting for the higher observed resistance. The lower differential resistance observed for p-type doped layers in both their virgin and high impedance states suggests that Schottky-barrier contacts are not required for the observation of the memory switching phenomenon in polysilicon.

Further experiments with doping variations confirm this hypothesis. The memory switching is observed in both n^+-n-n^+ and p^+-p-p^+ layers. For such layers, lower resistances in both the virgin and high impedance states are observed than if an intrinsic layer is used. The principal change brought about by the use of heavily doped layers adjacent to the metal contacts is an increase in the number of times which a device may be cycled between the low and high impedance states before catastrophic damage occurs.

The I-V characteristics of a single crystal n^+ silicon — undoped polysilicon layer — molybdenum device (structure of Fig. 1(b)) are presented in Fig. 4. Note that both the low and the high impedance states have a lower resistance if the n^+ single crystal substrate is biased negatively.

The upper electrode need not be molybdenum in order to observe memory switching. Chromium, aluminum and gold electrodes have been used as top contacts in place of molybdenum. In addition, tungsten, platinum and graphite probes have been used as point contacts instead of broad area electrodes. In all these variations of device structure memory switching was observed. However, the number of times the devices could be cycled between high and low impedance states before permanent damage occurred was dependent upon the top electrode material. Molybdenum and graphite contacts permitted the largest number of cycles, aluminum, chromium and gold, the fewest.

The I-V characteristics shown in Figs. 2-4 were obtained using triangular voltage pulses from a 120 Hz curve tracer. The devices may be transferred between states using shorter duration square pulses. Single-shot pulsing of a device to bring it from its high to its low impedance state transition required pulse lengths of 25-50 ns in order to accomplish the transition with certainty if the same voltage level was used as for the curve tracer induced switching. The actual transition time was much shorter (1-5 ns), but a random delay time between

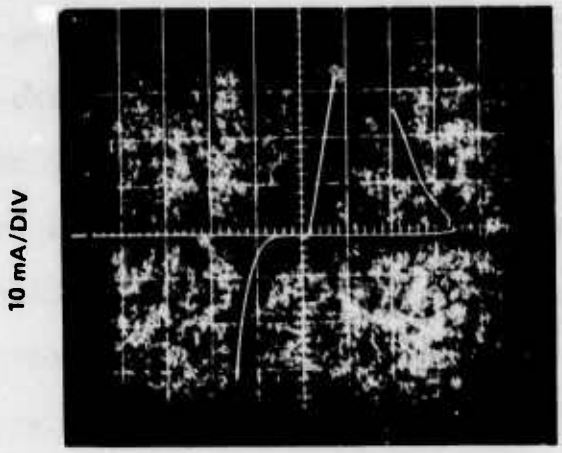


FIG. 4 Current-voltage of molybdenum – updoped polysilicon – n^+ single crystal silicon device for high and low impedance states. Positive sense of voltage corresponds to molybdenum biased positive and n^+ silicon substrate biased negative.

the start of the pulse to the actual time of transition was observed which was shorter for high pulse voltages, reminiscent of the behavior of amorphous memory diodes.[5] To ensure the accomplishment of the reverse switching from low to high impedance state, much longer pulses, from 10-25 μs, were required if the current level was the same as for the curve tracer induced switching.

If either the set or reset operation was accomplished by pulsing, then the device was more completely locked into its final state than it would have been using a curve tracer power supply at the same peak current and voltage. This result was somewhat surprising, since clearly less total power is dissipated in the device in single-shot pulsing than in multiple cycles of the curve tracer. The current and voltage levels of both the pulsed power supply and the sawtooth waveforms of the curve tracer were carefully calibrated to be certain that the peak current or voltage of the single-shot pulse was always less than the curve-tracer peaks. The "completeness" of the set or reset process was measured quantitatively by determining the minimum current (or voltage) which must be supplied by the curve tracer in order to "undo" the previous process.

Raising the device's temperature to 90-120°C caused a partial erasure of the low impedance state in 12-24 hours. Storage for 1-2 hours at 250°C resulted in complete erasure of the low impedance state. No change in state was observed if the devices were stored at 77°K. The turn-over voltage to negative resistance in the high impedance state increased about 10-20%, however, at 77°K. A higher input power is therefore required to bring the devices into their low impedance state. On the other hand, devices cooled to liquid nitrigen temperature required less power to reset back into their high impedance state than if the process was attempted at room temperature.

RADIATION HARDNESS

The device structure used to obtain the data of Fig. 2 was subjected to radiation tolerance tests by exposing the devices to 450 ns pulses of 10 MeV

electrons. When subjected to ionizing radiation at a rate of 10^8 rad (Si)/s (0.5 rad (Si) total dose), all devices which were not in their virgin state tended to revert to their low impedance state. Only two to three pulses were required to bring a device completely into its low impedance state regardless of whether a bias was or was not applied to the device during exposure. Applying 5-10 radiation pulses left all devices permanently locked in their low impedance state. The lack of radiation hardness is a major difference between these devices and at least some amorphous memory switches.[8] The radiation appeared to have no effect upon devices which were in their virgin state.

FILAMENTARY CONDUCTION AND DEGRADATION

Devices which have been brought to their low impedance state show clear evidence of filamentary conduction. If a sufficient number of set-reset cycles are accomplished (between 1-10^3, depending upon device structure), a localized breakdown region may be observed which is very similar in behavior and appearance to that described by Feldman and Moorjani in amorphous silicon layers.[3] Increasing the number of set-reset cycles increases the diameter of the spots. Limiting the power dissipated in each set or reset operation will delay, but not prevent, the cessation of memory switching. High values of series load resistance in the high-to-low impedance transition and low values of load resistance in the low-to-high impedance transition are useful for this purpose. At most 2×10^4 cycles have been observed using the structure of Fig. 1(a). Near the end of its useful life, higher voltages and current are required to cause switching, and the device is finally left permanently and unalterably in one of its impedance states (usually the low impedance state).

Even if localized breakdown cannot be observed microscopically after the first few switchings, it is still believed that localized breakdown is involved. Dividing the upper electrode in half by etching will always leave one

half of the device with a low impedance state resistance identical to that of the complete original device; the other half of the device will have a virgin state characteristic.

FILM STRUCTURE

The 1-2 μm thick silicon films deposited at 700°C on both molybdenum and single-crystal silicon were polycrystalline with a ⟨110⟩ preferred orientation as determined by x-ray diffraction. This is in agreement with the results of Nagasima and Kubota[7] for films deposited on SiO_2. However, these same authors report that films 0.1 μm thick had an amorphous structure as determined by electron diffraction, and it is possible to hypothesize that such an amorphous layer (which was not detectable by x-ray diffraction) was present in our films and was responsible for their switching behavior. Several experiments were carried out which suggest that an amorphous layer is not necessary for the memory switching.

The first experiment used 2 μm thick silicon films deposited on single-crystal silicon at 700°C. The wafer was divided in half for subsequent processing. One half was annealed at 1150°C for 30 min. in nitrogen before the top metal contact was applied; the other half of the wafer was treated as usual with no anneal. Nagasima and Kubota report that 10 min. heating at 1100°C of completely amorphous films is sufficient for crystallization.[9] Devices taken from both halves of the wafer showed essentially the same switching characteristics. However, the voltage required to erase the virgin state (a one-time event) was usually lowered by such an anneal.

In other experiments, 0.3 μm thick silicon layers were deposited on single-crystal silicon wafers at 700°C and 800°C. No evidence of a crystalline state was obtainable by x-ray diffraction, although this does not imply that the films were amorphous. However, following anneals at 900°C for two hours the films

deposited at 800°C did produce a diffraction pattern with a preferred ⟨111⟩ orientation. (Any tendency to also show a ⟨100⟩ orientation may have been masked by the ⟨100⟩ substrate.) The thin films deposited at 700°C which were not annealed could be recycled the fewest number of times (10-100) and had a low ratio between that resistance of the high impedance state and the low impedance state. The films deposited at 800°C (at which temperature Nagasima and Kubuto report polycrystalline films by examination using electron diffraction)[7] were more rugged and had a higher ratio between the impedance levels of the two states. The annealed films showed improved memory switching both for the 700°C and 800°C depositions. The 800°C deposited film, which was annealed at 900°C (which did show evidence of crystallizing by x-ray diffraction), could be cycled 500-1000 times and yielded the best memory switches. Thus, these experiments show a correlation between improved switching characteristics and a probable greater extent of crystallinity.

CONCLUSIONS

CVD deposited polycrystalline silicon films show a memory switching phenomenon when subjected to electric fields of the order of 10^4 V/cm, with filamentary conduction occurring in the low impedance state. The appearance of the phenomenon does not depend on a particular electrode material, although different electrode materials can cause variations in device ruggedness. We have found no evidence that memory switching requires the existence of an amorphous silicon sublayer within the active device.

The establishment of a filamentary conduction path occurs when the devices are removed from their initial high impedance state. This erasure of the virgin state is a one-time event and almost certainly involves a structural change in the layer. Subsequent switchings of the filamentary path between high

and low impedance states may well not require any further structural change, since it can be brought about by the dissipation of energy of only 5×10^{-6} J/gm (0.5 rad) of irradiated silicon. However, repeated electrically induced switchings do in fact cause further structural damage which ultimately degrades the device. The maximum number of cycles observed ($\approx 2 \times 10^4$) may not represent the upper limit to what might be obtainable with the use of either different electrode materials or more complex voltage pulse shapes for setting and resetting the device's states.

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APPENDIX D

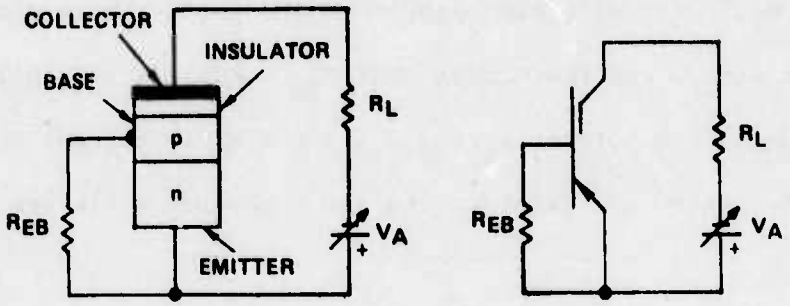
RADIATION RESISTANCE OF ICS DEVICES

I. INTRODUCTION

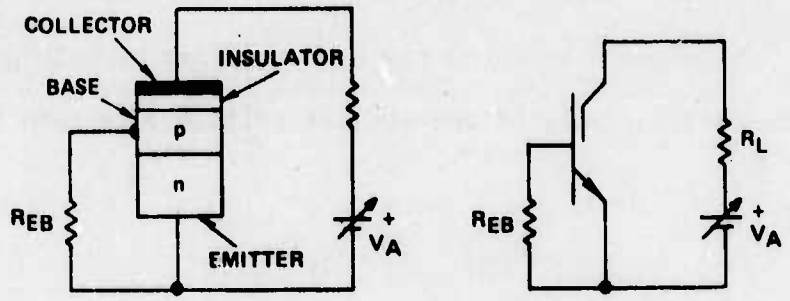
The inversion controlled switch (ICS) has been demonstrated as a memory device[1] since it can exist in either of two stable impedance states.[2,3] Illumination of the device with silicon band gap radiation has been shown to reduce the threshold voltage V_{TH}, the highest voltage which may be impressed upon the device in its high impedance state.[3] One therefore expects that irradiation of the device by any means which creates electron-hole pairs will lower the threshold voltage. This paper presents the first experimental data on the suppression of V_{TH} by high energy electron radiation. The sensitivity of suppresion of V_{TH} is found to depend upon which of various alternate device structures is used,[3] with one particular structure, a molybdenum-silicon oxynitride-p-n^+ device, showing rather interesting insensitivity to transient 1 meV electron irradiation.

II. CIRCUIT CONSIDERATIONS

The basic ICS circuit which can be used as a memory element is shown in Fig. 1, along with circuit symbols. The circuit symbols and motivation for the naming of the "emitter," "base," and "collector" regions of the device have been introduced previously.[3,4,5] Figure 2 illustrates typical current-voltage (I-V) characteristics. Binary logic states may be defined as "0," corresponding to the high impedance state and "1," corresponding to the low impedance state. In order to hold information in a



(a) M-INSULATOR -n -p



(b) M-INSULATOR -p -n 78-39

FIG. 1 Grounded emitter circuit diagram and structure of ICS device.
(a) M-I-N-P
(b) M-I-P-N

memory cell, the circuit parameters of Fig. 1 must be properly chosen. The applied voltage V must be less than V_{TH} or the device could not exist in its high impedance state. Similarly, the applied voltage must be greater than a critical value V_c, as defined in Fig. 2, or the device could not exist in its low impedance state.[2] V_c is obviously also a function of the load resistance R_c.[2] (V_c will also depend on the emitter-base shunt resistance R_{EB}[5] but we assume for the moment that $R_{EB} = \infty$). It is clear from Fig. 2 that the sustaining current I_s and V_s, the minimum current and voltage, respectively, which can exist in the low impedance state are related to R_L and V_c by

$$V_c = V_s + I_s R_L \tag{1}$$

under the assumption that the current in the high impedance state may be neglected. The above discussion may be summarized by noting that memory operation is possible only if the applied voltage V is such that

$$V_c(R_{EB}) < V < V_{TH}(R_{EB}) \tag{2}$$

Since both I_s and V_{TH} can depend quite sensitively, in some ICS devices, upon R_{EB},[5] the explicit functional relationship is retained in the inequality of Eq. (2).

III. DEVICE STRUCTURES

The basic structures investigated are diagrammed in cross section in Fig. 3. The devices had circular symmetry with an annular base contact for three terminal devices. Insulator layers were formed using silicon-

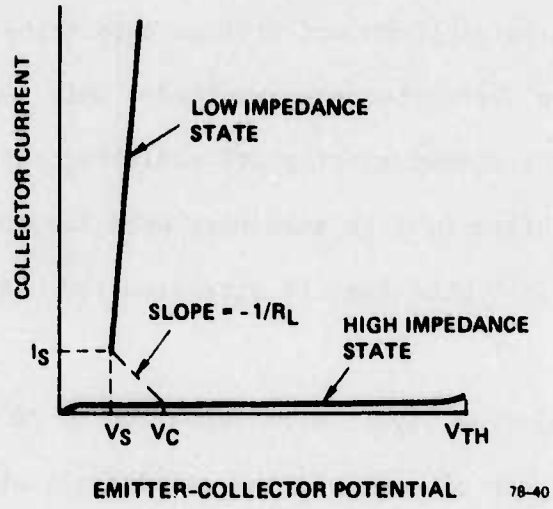


FIG. 2 Current voltage characteristics of ICS and definition of critical currents and voltages.

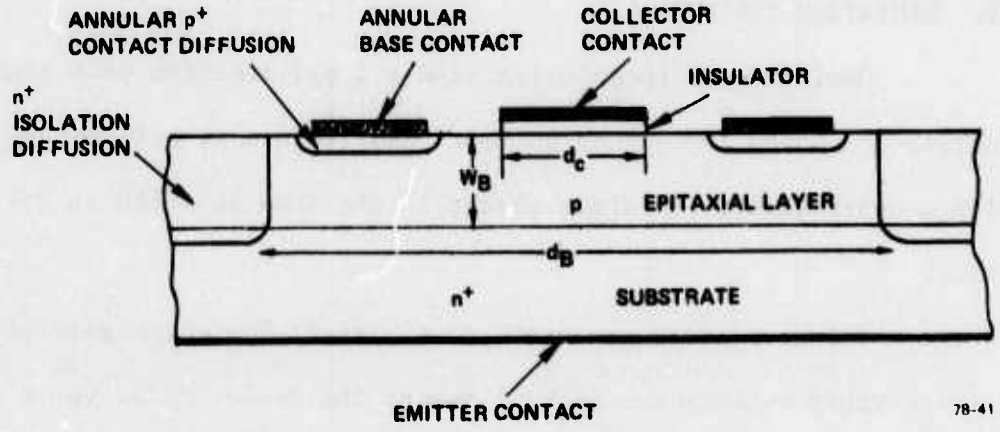


FIG. 3 Cross sectional view of typical ICS device studied, drawn for special case of M-I-P-N^+ device with epitaxially grown junction.

rich, silicon nitride (index of refraction = 1.8 at 5460 Å), silicon oxynitride (index of refraction = 1.68 at 5460 Å), SiO_2 and polysilicon. Metal-insulator-n-p^+, metal-insulator-p-n^+ and metal-insulator-p^+-n-n^+ devices were studied both for SiO_2 and silicon-rich silicon nitride insulators. For the insulating polysilicon and silicon oxynitride insulators, only the metal-insulator-p-n^+ variation was examined. Only the structure with the oxynitride insulator showed substantial radiation resistance. For this reason slight variations in this structure were fabricated with only two terminal contacts (the base contact diffusion and base contacts of Fig. 3a were omitted).

The oxynitride layers were deposited at 700°C in a cold wall reactor using 15 ℓ/min of argon as the carrier gas with 250 cm^3/min of 1% silane in argon, 250 cm^3/min of NH_3 and 35 cm^3/min of N_2O. Wafer preparation followed the procedure previously described.[2]

IV. RADIATION TESTING

Devices were irradicated with a 1 meV electron beam from a LINAC accelerator, using 100-450 ns pulses. Radiation dose rate was monitored using a calibrated p-i-n diode placed in the same location as the test device.

The devices were mounted on a circuit box which permitted adjustment of the circuit resistances without moving the device relative to the electron beam. Most tests were performed with the device 10 cm from the exit port of the accelerator where the beam area is of the order of 4 cm^2 so that accurate relative posioning of the test device and calibrated p-n diode is not critical. For obtaining the highest dose rate of the order of 10^{10} rads (Si)/s, a closer placement of 3 cm was necessary where the beam diameter is

much smaller. The position of both the test device and p-i-n diode was chosen by placing them just behind a plastic sheet whose previous exposure to the beam had developed a visible spot.

Tests were performed to determine the maximum dc voltage $V_M(R)$ that could be applied to a device and a series-connected load resistor R_L which would still prevent the device from switching from its high to low impedance state when irradiated with a radiation dose rate R expressed in units of rads (Si)/s. These tests were usually repeated for a variety of circuit configurations.

V. EXPERIMENTAL RESULTS AND DISCUSSION

Typically observed results of the radiation tests are illustrated in Fig. 4 which presents the variation in the maximum voltage $V_M(R)$ which can be applied to two different ICS structures as a function of the logarithm of the radiation dose rate without having the radiation initiating a transition from the high to the low impedance state of device. It is obvious that the two different types of devices have a quite different dependence of $V_M(R)$ upon R. The molybdenum-silicon oxynitride-n-p^+ clearly has a less sensitive dependence upon the radiation dose rate than does the molybdenum-polysilicon-p-n^+ device. It is presumed that the differences in V_A for the 3 cm and 10 cm window-to-device separation of the $M/SiO_xN_y/p\text{-}n^+$ device is due to errors in normalizing the radiation dose rate (alignment error or saturation of the p-i-n diode); the device's I-V characteristics did not change as a result of the radiation tests. Two other features of the curves of Fig. 4 are the more rapid decrease of $V_M(R)$ at lower values of R and the relative saturation of $V_M(R)$ at higher values of R.

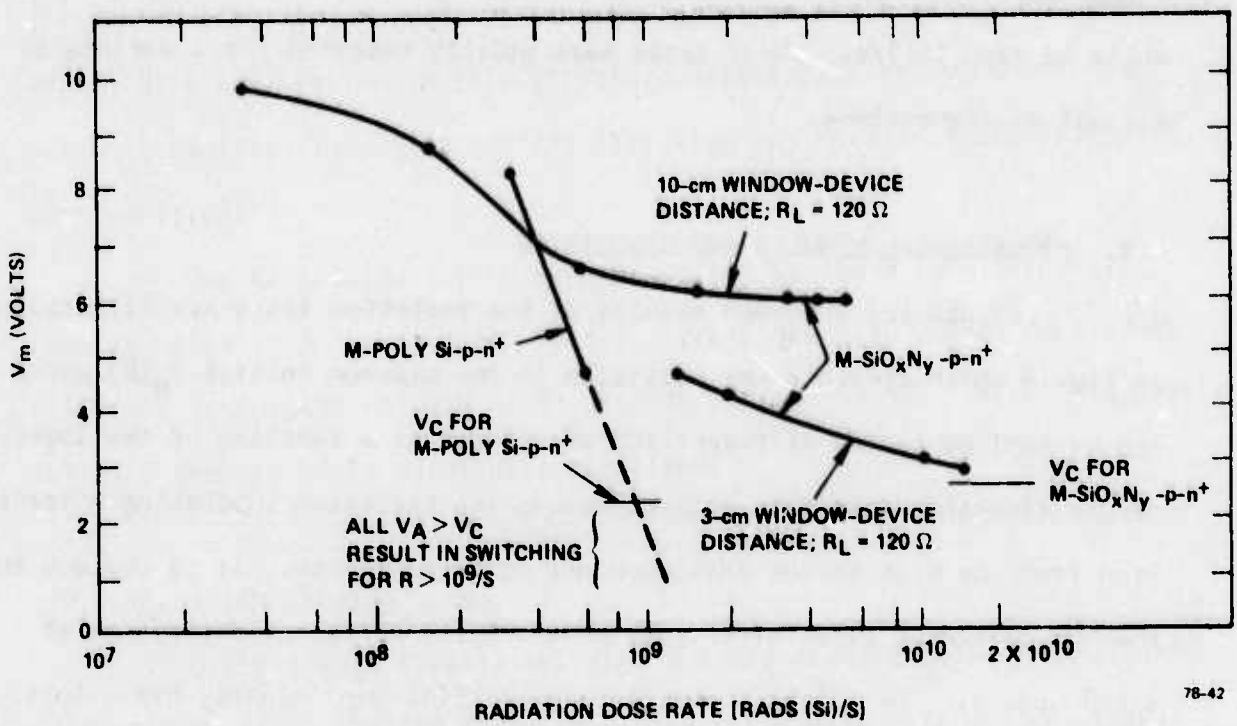


FIG. 4 Maximum voltage V_M which can be applied to devices and load resistor which permits device to remain in high impedance state as a function of applied radiation dose rate for M-polysilicon-p-n^+ device and type "A" M-SiO_xN_y-p-n^+ device.

A qualitative explanation of these data of Fig. 4 is obtained from a comparison with the behavior of the threshold voltage V_M of three terminal versions of these devices as a function of applied base current. The primary effect of the electron irradiation is the creation of electron-hole pairs in the semiconductor; the primary effect of base current is the injection of minority carriers into the base region of the device. The implied equivalence of these processes assumes that the major result of the pair creation by electron irradiation is the accumulation of minority carriers near the collector of the device.

The applied switching voltage V_A and the base current I_B is presented in Fig. 5 for both the polysilicon and the silicon oxynitride device. Since both device structures have equal collector and emitter areas, and both emitters are much more heavily doped than the base regions, the current scale of Fig. 5 is a good approximation to the relative rate of minority carrier injection for both devices. Inspection of these data therefore suggests that the polysilicon device should be more easily switched from its high to low impedance state by radiation than the oxynitride device, as is observed.

The correspondence between the relative scales (rads(Si)/s for Fig. 4 and current for Fig. 5) can be approximated by the following considerations. The number of electron-hole pairs produced per second per cm^3 of silicon will be given by

$$N = R \times (4.43 \times 10^{13}) \quad . \tag{5}$$

The effective volume V in which they are produced is taken to be the product of the collector area (1.25×10^{-4} cm^2) and the base width (4×10^{-4} cm).

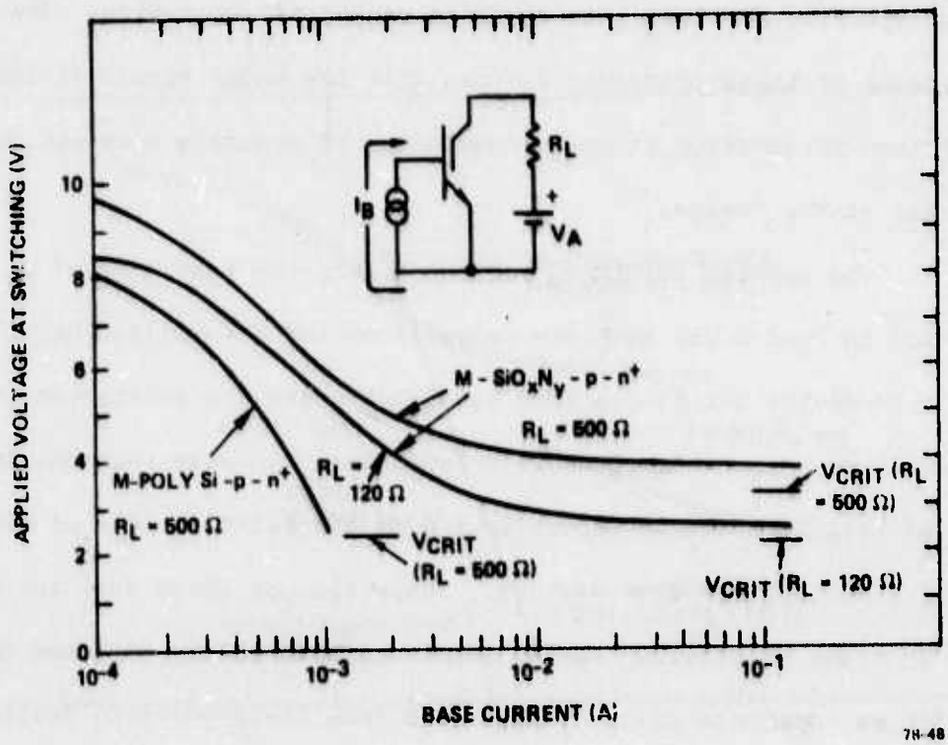


FIG. 5 Voltage applied to device and series load resistance at switching as a function of applied base current.

This assumes that pairs created in the emitter area will recombine before crossing the emitter junction and that most pairs produced outside the collector area will recombine before diffusing to the collector depletion zone. The primary current produced by the radiation will therefore be

$$I_R = q\ R\ V(4.43 \times 10^{13}) \quad .$$

This current should be compared to a base current which is smaller than the applied base current by a factor of 1/36, since, assuming uniform emitter current density, only this fraction will reach the collector because the ratio of collector to emitter area is 1:9. The observed base current gain of these devices (measured approximately at V_{TH}) is ≈ 4, so for an "ideal" device (with equal collector and emitter areas), the radiation produced at R rads(Si)/s therefore should be comparable to the effect of a base current in the real device equal to

$$I_B = 36\ qRV\ (4.43 \times 10^{13}) \qquad (6)$$

or

$$I_B = 1.28 \times 10^{-11}\ R$$

If, for example, $R = 10^9$ rads (Si)/s, the equivalent base current is 1.28 mA. From Fig. 4, an applied radiation dose rate of 10^9 rads/Si)/s suppress V_{TH}, to about 4-6 V; from Fig. 5, a base current of 2 mA suppress V_M to about 5 V. The approximate correlation between equivalent base current and R is therefore not completely unreasonable.

Most other structural variations investigated behaved under irradiation in a manner at least qualitatively predictable from knowledge of

their $V_{TH}(I_B)$. For example, M-SiO_2-n-p^+ devices which have an extremely sensitive suppression of their threshold voltage by base current[5] could not be kept in their high impedance state for radiation dose rates above 5×10^8 rads/s for any applied bias above V_C.

Another structure, a M-SiO_2 p^+-n-n^+ device, whose base region was produced by diffusion, behaved under irradiation in a manner which is understandable on the basis of the above considerations. Even though this device had only a weak suppression of its threshold voltage when base current was applied, the device was fairly sensitive to electron irradiation with dose rates above 10^9 rads/s causing the device to switch to its low impedance state at any applied voltage above V_C. The base p^+ region of this device was doped almost as heavily as the emitter, however. Thus, the small depression of V_{TH} with base current probably reflects a low efficiency of injection of minority carriers into the base rather than some inherent insensitivity of the device's threshold voltage to increased minority carrier density in the collector region.

VI. EFFECT OF CIRCUIT AND DEVICE VARIATIONS ON RADIATION HARDNESS

The SiO_xN_y insulator devices which were the most radiation resistant structures were further examined to include the effects of different circuits and variation in device structure upon radiation hardness. The first of these experiments involved nothing more than the change of load resistance in a simple two-terminal connection. The data of Fig. 6 were obtained using another variant of the M-SiO_xN_y-p-n^+ structure which was fabricated for the sole purpose of checking that the radiation hardness was a reproducibly obtainable behavior of this basic structure. The tested devices were made within a simple two-terminal format in order that device fabrication be expedited.

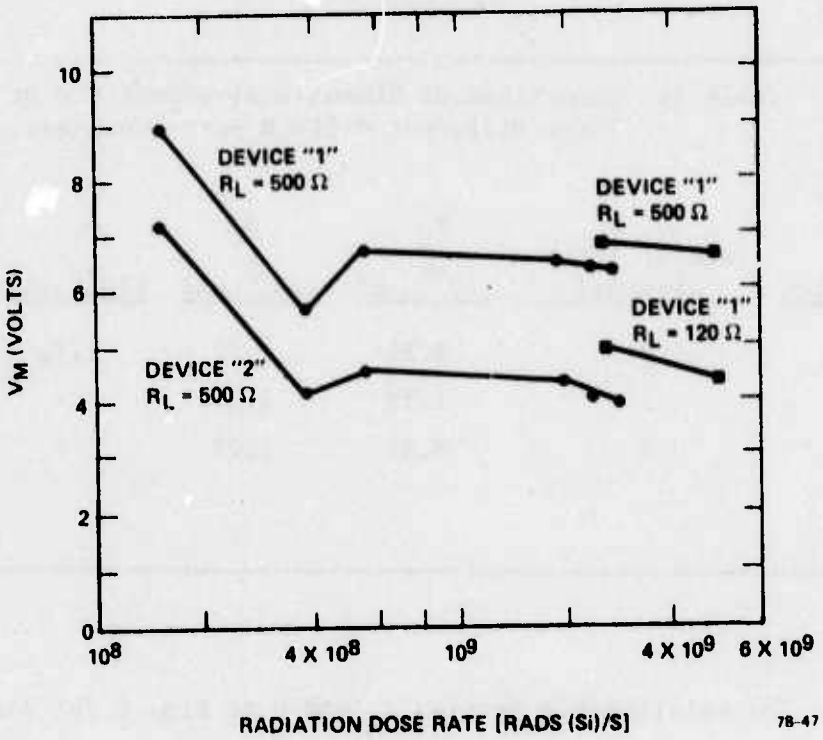


FIG. 6 Maximum voltage V_M for type "B" SiO_xN_y-p-n^+ device as a function of radiation dose rate.

Table i lists the various dimensional parameters of the devices used to obtain the data of Figs. 4 and 6. All these structures were fabricated from similar starting p/n^+ silicon wafers. The emitter and collector diameters d_E and d_C, and the inner and outer diameters d_1 and d_2 of the base contact diffusion are defined in Fig. 3.

Table 1. Comparison of dimensional parameters of three different M-SiO_xN_y-p-n^+ devices.

Device	Two- or Three-Terminal	d_E (10^{-2} cm)	d_C (10^{-2} cm)	d_1 (10^{-2} cm)	d_2 (10^{-2} cm)
A	3	3.81	1.27	1.78	2.54
B	2	1.78	1.27	-	-
C	2	3.81	1.27	-	-

The relationship between V_M and R of Fig. 6 for structure B is seen to be qualitatively similar to that obtained for the three-terminal structure A shown in Fig. 4. The relative minimum value of V_M at $R = 4 \times 10^8$ rads(Si)/s is not observed in Fig. 4, however, and occured for all structures tested on the date these data were obtained. No explanation is available for this.

The two different devices "1" and "2" represent the widest variation in threshold voltages available from this run. Device "1" with a threshold voltage of 10 V was typical of the run; device "2" with a threshold voltage of 8 V was selected as the device with the lowest threshold voltage of the run. Note that V_M, the maximum voltage which can be applied to the device, and the load resistor with the radiation causing the device

to switch to the low impedance state track each other through the range of applied radiation dose rates. The data obtained at the highest dose rates (marked by square symbols) were obtained on different days. The slight differences between this data and that obtained at lower R may be caused only by error in calibration of the LINAC's output radiation. The change in V_M upon changing R_L from 500 to 120 Ω is believed to represent a real effect/ The device was not moved in changing R_L and one set of data was obtained immediately after the other.

The effect of varying R_L on V_M can be explained by an examination of three terminal device characteristics of the related three terminal devices. Note that the voltage required to cause switchings as a function of applied base current shown in Fig. 5 explicitly depends upon the load resistance. The difference between V_A(500 Ω) and V_A (120 Ω) at high values of I_B is about 1.5 V; the difference in V_M (500 Ω) and V_M (120 Ω) is about 2.5 V at high values of R. This approximate argument is probably all that can be expected considering the fact that the two devices ("A" and "B" of Table 1) do not have identical two-terminal I-V characteristics.

The reason that V_A required for switching differs so much for R_L = 500 Ω and R_L = 120 Ω, as illustrated in Fig. 4, involves the details of conduction mechanism through the silicon oxynitride and such a discussion is beyond the scope of this paper. But it is useful to more explicitly discuss this difference with reference to the actual I-V characteristics of the device which are shown in Fig. 7a and 7b for R_L = 120 Ω and R_L = 500 Ω, respectively. The I-V characteristics, strictly within the high impedance state, are identical for both values of load resistance. The value of $V_A(I_B, R_L)$ for R_L = 120 Ω exceeds that of V_{TH} (I_B) because of the finite current carried in the high impedance state. Referring to Fig. 8, it can be

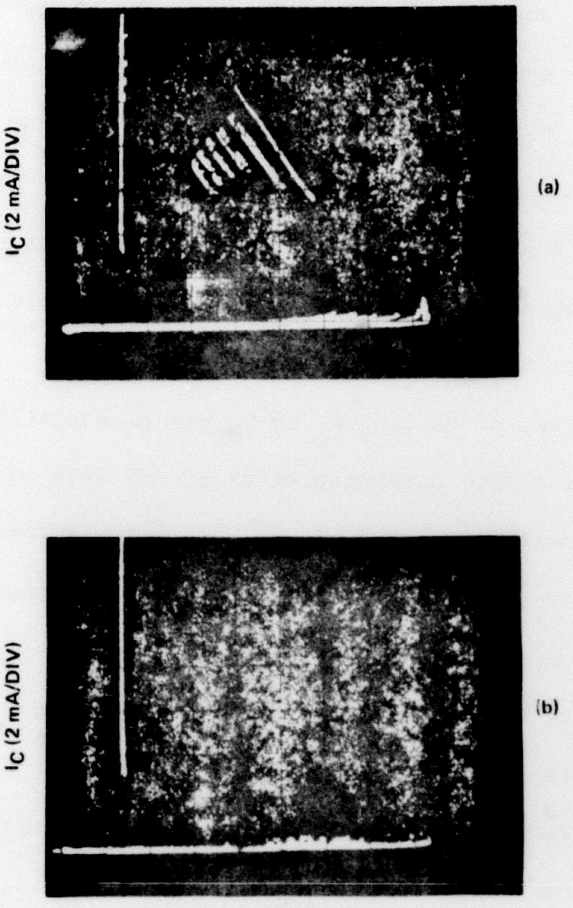


FIG. 7 Current voltage characteristics of type "A" M-SiO_xN_y-p-n^+ device. Note differential negative resistance characteristics only when R_L = 500 Ω.
(a) R_L = 500 Ω.
(b) R_L = 120 Ω.

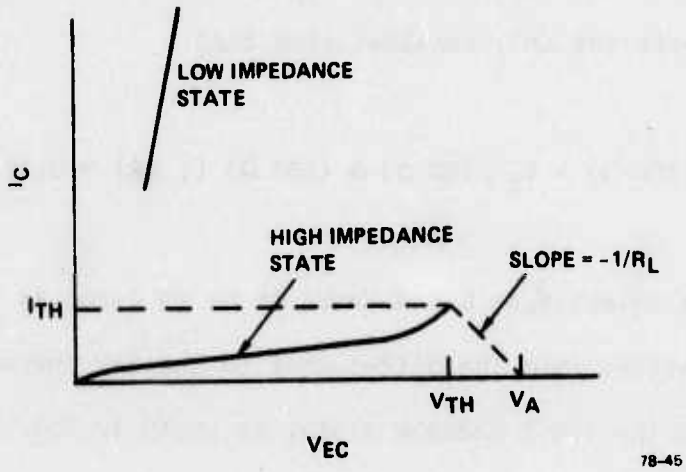


FIG. 8 I-V characteristics of high impedance state illustrating relation between threshold voltage V_{TH} and applied voltage V_A at switching for device with I-V characteristics as in Fig. 7b.

seen that

$$V_A = V_{TH} + I_{TH} R_L \tag{7}$$

where I_{TH} is the maximum current carried in the high impedance state. Note that V_{TH} is independent of R_L and is defined as the maximum voltage across the device itself which can exist in the high impedance state.

Now at high values of I_B, $I_{TH} \approx 1$ mA. Thus, one would expect that if this were the only consideration that

$$V_A\ (500\ \Omega) - V_A\ (120\ \Omega) \approx (380\ \Omega)\ (1\ \text{mA}) = 0.38\ \text{V} \tag{8}$$

whereas ΔV_A is observed, as noted above, to be as large as 2 V. The larger value of ΔV_A arises from the differences in the I-V characteristics of the devices beyond the low impedance state, as shown in Fig. 7b, where there are differential negative resistance (DNR) characteristics of the device between the low and the high impedance states which are only apparent when $R_L = 500\ \Omega$.

The DNR characteristics are quite different from the "intermediate impedance state" previously defined[3] in several respects: The true intermediate state has a positive differential resistance whose differential resistance is independent of the load resistance and whose voltage is independent of I_B. The differential resistance of the peculiar state of Fig. 7b is equal to $-R_L$ for $400 < R_L < 3000\ \Omega$ and its voltage shifts with changes in I_B as shown. More importantly, transitions to the true intermediate state are latching transitions in that unless the collector voltage is lowered, the device will remain in the intermediate state even if an applied base current which initiated the transition is removed. Transition to the DNR states of Fig. 7, on the other hand, are nonlatching

transitions unless the collector current exceeds the upper limit sown, i.e., $I_C \gtrsim$ 9 mA for I_B = 0 and 0.1 mA.

Those DNR states therefore act as a block for transitions into the low impedance state. Much greater collector current must therefore be generated to cause the device to make a transition to the low impedance state. Use of such a high value of R_L so as to cause these DNR states to appear will slow down transitions to the low impedance state even more than would be expected by an increase in collector time constants, but one could design a memory circuit which has a different effective load resistance for holding information than it does during writing operations. The blocking action of these DNR states may therefore be of great practical utility.

Further changes in sensitivity to radiation are observed when electrical connections are made to all three terminals of the device. Electrical connection to the base terminal is desirable for memory circuit applications and in such circuits there is often an effective resistance or p-n junction diode connected between the base and emitter terminals.[1] The basic effect of adding a shunt conductance between the emitter and base terminals is shown in Fig. 9 for two other devices with a M-SiO_xN_y-p-n^+ structure similar to that used to obtain the data of Fig. 4. Note that adding a shunt conductance, as shown in the insert to Fig. 9, increases V_M for either value of R_L. Also shown is V_M for a similar device which had bonded to it mount a shunt diode, according to the second circuit shown in the insert. This shunt diode was irradiated, of course, along with the device itself.

The effect on radiation resistance of adding a shunt conductance between emitter and base can be qualitatively explained by considering the effect on the quiescent current-voltage characteristics of the device. The

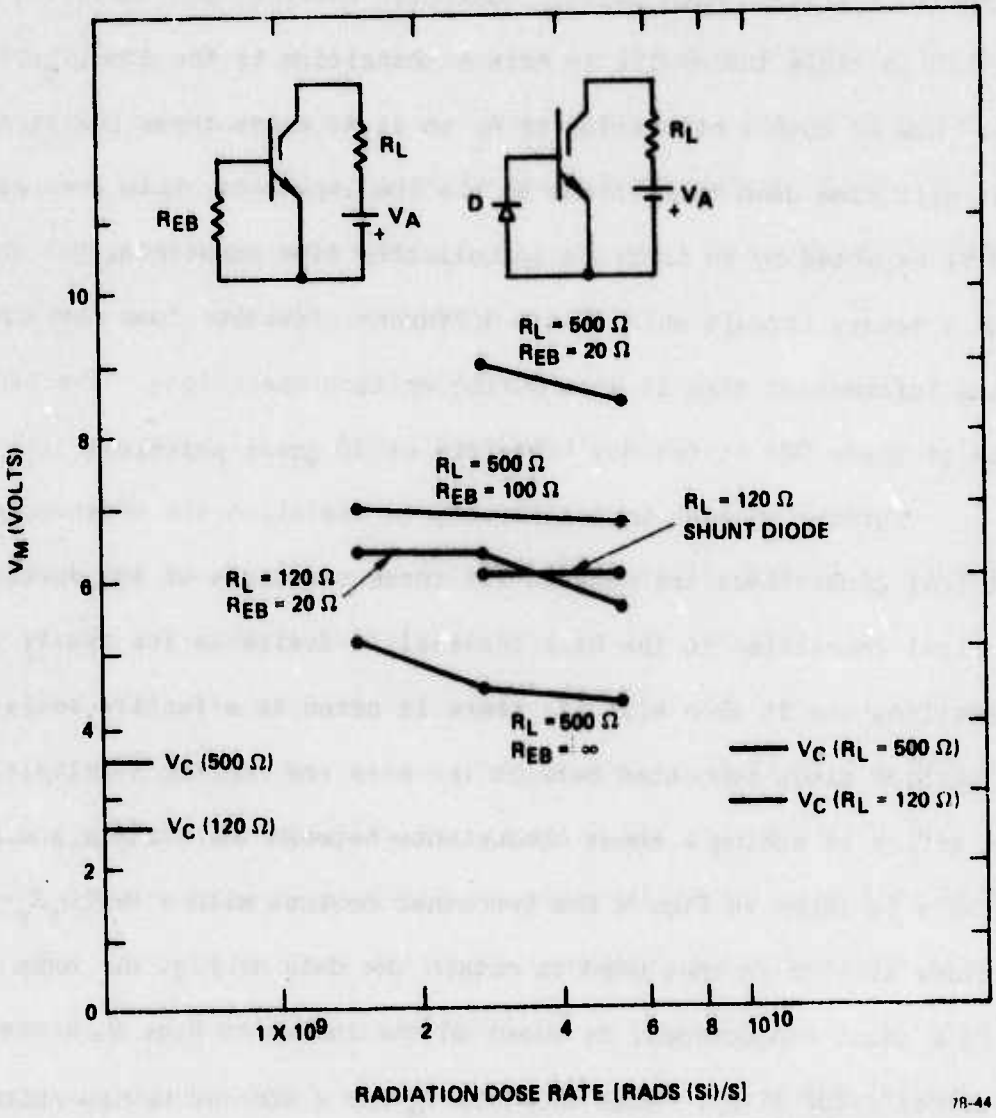


FIG. 9 V_M as a function of radiation dose rate for type "A" Mo-SiO_xN_y-p-n^+ devices for several three terminal circuit arrangements.

major effect is to increase the devices' threshold voltage[5] by tending to lower the emitter-base junction bias. This causes decreased injection[5] and, perhaps, more importantly, a decrease in the regenerative processes emphasized by Simmons and coworkers[6] in which the number of base majority carriers which cross the junction is multiplied to further increase the number of base minority carriers which reach the collector. The external connection to the base terminal also permits a new avenue of escape of minority carriers that might otherwise diffuse to the collector depletion zone. For these particular devices, the critical voltage V_C, the minimum voltage which must be applied to hold the device in its low impedance state, was not affected much by emitter-base shunt conductance,[5] and therefore the increase in V_M shown in Fig. 9 represents a real net gain in the allowable range of applied V.

Finally, a third variation of a two-terminal structure was tested. This was the device structure "C" of Table 1. As shown in Fig. 10, this device was scarcely affected by radiation up to the maximum radiation dose rate available with the exception of the anomalous reduction in V_M at 4×10^8 rads(Si)/s. This insensitivity to radiation cannot be explained because structural variations of this type of device have not been studied except in this experiment. (Except for the radiation immunity, these particular types of devices have not been the best performing memory devices, largely because of the insensitivity of their threshold voltage as a function of base current.) However, one may be suspicious that the enlarged SiO_2 p-type Si interface near the collector region acts as an efficient recombination surface for minority carriers, thus reducing the total flux of minority carriers which reach the collector. In support of this hypothesis is the observation that the threshold voltage is higher for this structure than either of the "A" or "B" variations.

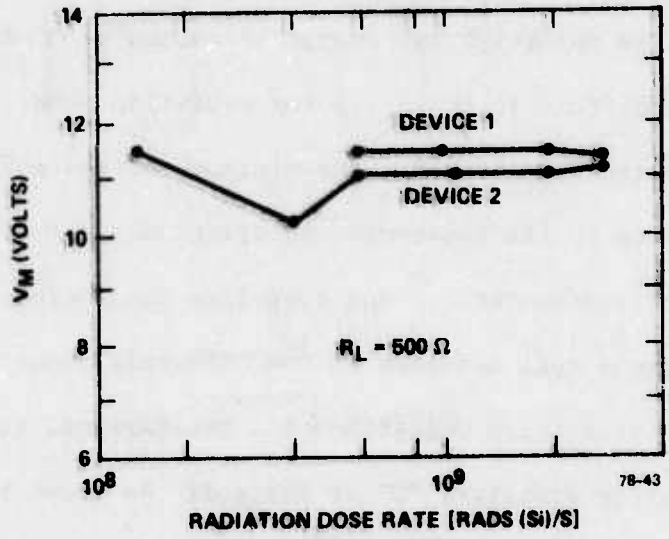


FIG. 10 V_M as a function of radiation dose rate for type "C" Mo-SiO_xN_y-p-n^+ devices.

VII. SUMMARY AND CONCLUSIONS

The sensitivity of ICS devices to high energy electron radiation has been measured for the first time. The general behavior of the device under radiation can be explained by considering how the device behaves under three-terminal biasing without radiation. The less sensitive the reduction in device threshold is to applied base current, the less sensitive the device is to radiation. Both the application of base current and the irradiation of the device will increase the minority carrier flux which reaches the collector depletion zone which accounts for the commonality of their effects. The reduction in sensitivity to radiation caused by a shunt conductance across the emitter-base terminals is similarly explained by a reduced total collector of minority carriers.

The particular structural variation of ICS devices which was found to have the greatest resistance to radiation was a Mo-SiO_xN_y-p-n^+ structure. All variations in this structure which used the same insulator material showed high radiation immunity.

The use of silicon oxynitride as the insulator material does impose a performance penalty because of the higher power requirements. Use of SiO_2 or polysilicon insulator materials, for example, would permit a collector sustaining current density of the order of 1.6 A/cm^2. For the silicon oxynitride insulator, however, the sustaining current density is of the order of 10-20 A/cm^{-2}. The minimum power required to hold a device in the low impedance state is given by

$$P_{MIN} = I_C^2 R_L + V_S I_C \quad . \tag{9}$$

For a polysilicon or SiO_2 device with V_S = 1.5 V and R_L = 120 Ω and a

collector area of 1.25×10^{-9} cm^2, this minimum power is 0.3 mW. For the oxynitride device of the same dimension the minimum power is 3.5 mW. The increased power required to hold information in a silicon oxynitride insulator device is the primary penalty which must be paid for radiation hardness in an ICS memory circuit.

The fact that higher base current densities must be used to suppress the threshold voltage in order to select a given device within a memory array for transition to the low impedance state is another penalty which is incurred by use of the silicon oxynitride insulator. Base current densities approximately ten times as large must be used to suppress the silicon oxynitride device's threshold voltage to the same level as that of an SiO_2 polysilicon device. The fabrication and operation of a silicon oxynitride memory array is conceivable, however, with the circuit being immune to radiation dose rates in excess of 10^{10} rads/s.

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